



Epitaxial growth of radial Si *p-i-n* junctions for photovoltaic applications

Jinkyong Yoo,^{1,a)} Shadi A. Dayeh,^{1,2} Wei Tang,^{1,3} and S. T. Picraux^{1,a)}

¹Center for Integrated Nanotechnologies, Los Alamos National Laboratory, Los Alamos, New Mexico 87545, USA

²Department of Electrical and Computer Engineering, University of California San Diego, La Jolla, California 92093, USA

³Department of Materials Science and Engineering, University of California Los Angeles, Los Angeles, California 90095, USA

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Achieving high quality radial junctions in nanowire arrays with controlled doping profiles is critical for their potential photovoltaic applications. We present a low temperature epitaxial growth process for silicon radial *p-n* and *p-i-n* junction arrays on top-down fabricated nanowires using silane-based chemical vapor deposition. Epitaxial growth on [111] oriented nanowires of ~ 300 nm diameter and up to $10 \mu\text{m}$ in length exhibits well-defined, single crystalline {110} faceted surfaces at temperatures as low as 710°C . The growth rate G at 810°C for intrinsic Si is greater than that for heavily B- and P-doped Si ($G_i > G_p > G_n$). Faceted growth morphology at the tip of the nanowires results in well-defined “match-head” structures for undoped and B-doped growth. Preliminary photovoltaic device arrays of $\sim 4 \times 10^4$ nanowires based on our radial epitaxial *p-i-n* junction growth approach achieve solar energy conversion efficiencies of 10% under AM 1.5 G illumination. © 2013 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4794541>]

Silicon (Si) technology has continued to evolve rapidly in the area of three-dimensional (3D) structures and associated processing advances for device applications. One area of widespread current interest is the fabrication of vertical nanowire (NW) and microwire (MW) arrays with radial junctions to realize low-cost, high-performance devices for photovoltaic (PV) energy conversion.^{1–8} Si radial *p-n* junction vertical arrays are of particular interest as building blocks for high-performance PV cells, due to their enhanced light absorption while using relatively little Si and to the resulting orthogonalization between the light absorption and photogenerated carrier extraction directions.^{7,9}

Reliable and high-performance Si PV devices based on radial *p-n* junction arrays require high structural quality and spatial control of the electrical doping concentrations, with well-defined interfaces between *n*- and *p*-type regions. Previously, radial *p-n* junction arrays have been often fabricated by preparation of a vertical core material of one conductivity type and subsequent formation of an outer layer of opposite electrical type by dopant diffusion^{2,10} or ion implantation.³ Dopant diffusion, which is typically based on deposition of dopant-containing glasses on the surface of Si pillars, is a convenient method for *p-n* junction formation; however, it requires high temperatures and tends to give broad, graded *p-n* junctions. The resulting doping concentration profiles and junction depths in radial junctions are difficult to control and generally less than optimal for PV charge collection. Ion implantation is capable of better control of the dopant concentration profiles and more abrupt spatial distributions. However, ion implantation is a line of sight process and is not well suited to the radial conformal doping of dense high aspect ratio 3D arrays.

In contrast, epitaxial growth of single crystalline Si shells on vertical NWs or MWs allows the formation of conformal

and abrupt *p-n* junctions with highly controlled doping profiles over a wide range of dopant concentrations. An additional advantage of shell growth is the ability to form radial *p-i-n* junctions to tailor the absorption volume for a wide range of minority carrier diffusion lengths and therefore extend design options for improving PV device performance. However, the majority of studies of shell growth on Si NWs have shown amorphous, polycrystalline, or highly defected shells, which are not appropriate for high-performance Si PV applications.^{1,11–14} Single crystalline Si shells have been obtained by deposition of amorphous shell followed by thermal annealing to attain crystallinity¹¹ and by high temperature growth ($>900^\circ\text{C}$).¹⁵ On the other hand, a low temperature, high crystalline quality shell growth process allowing arbitrary doping profiles is highly desirable, because high temperature growth processes can introduce auto-doping, solid-state diffusion, and segregation effects and are typically not compatible with envisioned solar cell applications involving low-cost substrates.^{4,5,7,15} Only one report involving a single Si NW PV lateral device with single crystal Si core-shell structure has been carried out using lower temperature epitaxial shell growth,¹⁶ with no prior reports on PV devices made through epitaxial growth of radial junctions on vertical NW arrays.

The relative lack of single crystalline Si radial shell growth on NW arrays at low temperatures and minimal thermal budgets, combined with the importance of epitaxy at small scales for high performance device processing, motivated the present study of intrinsic and doped Si epitaxial radial growth on NWs. Radial growth at nanometer dimensions may be expected to involve a significant density of surface steps as well as the formation of multiple facets around the NW radius, which may lead to additional constraints for radial epitaxial growth on NWs and differences from conventional planar Si epitaxy. Here, we report the study of undoped and heavily *n*- and *p*-doped Si radial shell growth at temperatures of 670 to 810°C . We demonstrate well-defined faceted growth behavior at these nanoscale dimensions,

^{a)}Authors to whom correspondence should be addressed. Electronic addresses: jyoo@lanl.gov and picraux@lanl.gov.

observe the transition from amorphous and polycrystalline to epitaxial growth with increasing growth temperature, show the influence of dopants on reducing epitaxial growth rates, and achieve single crystalline Si radial p - n and p - i - n junctions. Further, we illustrate the efficacy of controlled low-temperature epitaxy by demonstrating PV efficiencies as high as 10% for NW cell arrays, values exceeding or comparable to the best previously obtained.^{3,5,6}

Arrays of vertical Si NW cores were formed by top-down fabrication using a combination of deep reactive ion etching (DRIE) and inductive coupled plasma (ICP) etching and passivation in a Bosch etch process to prepare epitaxy-ready radial shell growth. Figure 1(a) shows the scheme of preparation of the core Si NWs. Lithographic techniques (both e -beam lithography and photolithography) were used to form a patterned dot array etch-mask on Si (111) substrates consisting of a 1 μm thick SiO_2 layer with and without a thin top Ni/Ti layer (100/10 nm). After lift-off, the SiO_2 underwent ICP etching followed by Si Bosch etching with Ni/Ti/ SiO_2 nanodots acting as etch masks. Precisely controlled Si pillar arrays in the range of 300 to 1000 nm pillar diameter with lengths from 3 to 10 μm and spacings of 1 to 5 μm were fabricated (see the scanning electron microscope (SEM) image of an as-etched array in Fig. 1(b)). The SiO_2 etch mask was then removed by wet etching technique and residual Ti and Ni metals were cleaned by a standard RCA cleaning process. One to three dry oxidation steps at 1000 $^\circ\text{C}$ followed by dilute HF striping were carried out to further reduce the NW diameter to a desired value, remove the slight scalloped features left by the Si Bosch etching process on the NW sidewalls (see Fig. 1(c)), and provide an epitaxy-ready growth surface. Alternatively, we have also demonstrated that a wet etch process (1:1:20 nitric acid, hydrofluoric acid, H_2O solution giving 2 nm/min) can be used

for an all low-temperature process. Figure 1(d) shows a single row of the vertically aligned Si NWs with dimensions of 210 nm diameter, 8.8 μm length, and 1.5 μm pitch prior to etching. The wet etch or oxidation and strip procedure following the Si Bosch etch process was an essential step for epitaxial Si growth to prevent the scalloped etched surface from inducing an uncontrolled nucleation followed by polycrystalline growth. Figure 1(d) shows the smooth and rounded epitaxial growth-ready Si NW surface after three repeated surface oxidation and etching processes. An additional advantage of the surface smoothening process is the capability to precisely control the NW diameters and to form larger aspect ratios (>20) and smaller diameters (<200 nm) than were possible by Bosch etching alone. The Si radial shell growth on the epitaxy-ready Si NW cores was then carried out by low-pressure chemical vapor deposition (LPCVD) in a cold wall reactor using 50% SiH_4 in H_2 as the precursor, B_2H_6 as the p -type dopant source, and PH_3 as the n -type dopant source, both diluted in H_2 at 100 ppm and 5000 ppm, respectively. LPCVD at approximately 15 mTorr total chamber pressure with dopant precursor to SiH_4 gas ratios of 1.32×10^{-5} for B_2H_6 and 1.16×10^{-4} for PH_3 allowed low temperature epitaxial Si growth and uniform shell deposition. Approximate dopant concentrations were determined by 4-point probe measurements on epitaxial layers grown on planar reference samples under the same conditions and ranged from 1 to $3 \times 10^{19}/\text{cm}^3$.

For epitaxy, temperature is a critical parameter in controlling the growth behavior. Figures 2(a)–2(d) show high resolution transmission electron micrographs (HRTEMs) of NWs after the growth of undoped Si radial shells as a function of growth temperature from 610 to 810 $^\circ\text{C}$ for a fixed time of 3 min. At 610 $^\circ\text{C}$, the growth is polycrystalline with extremely small grains and some regions of amorphous Si. At 670 $^\circ\text{C}$, a

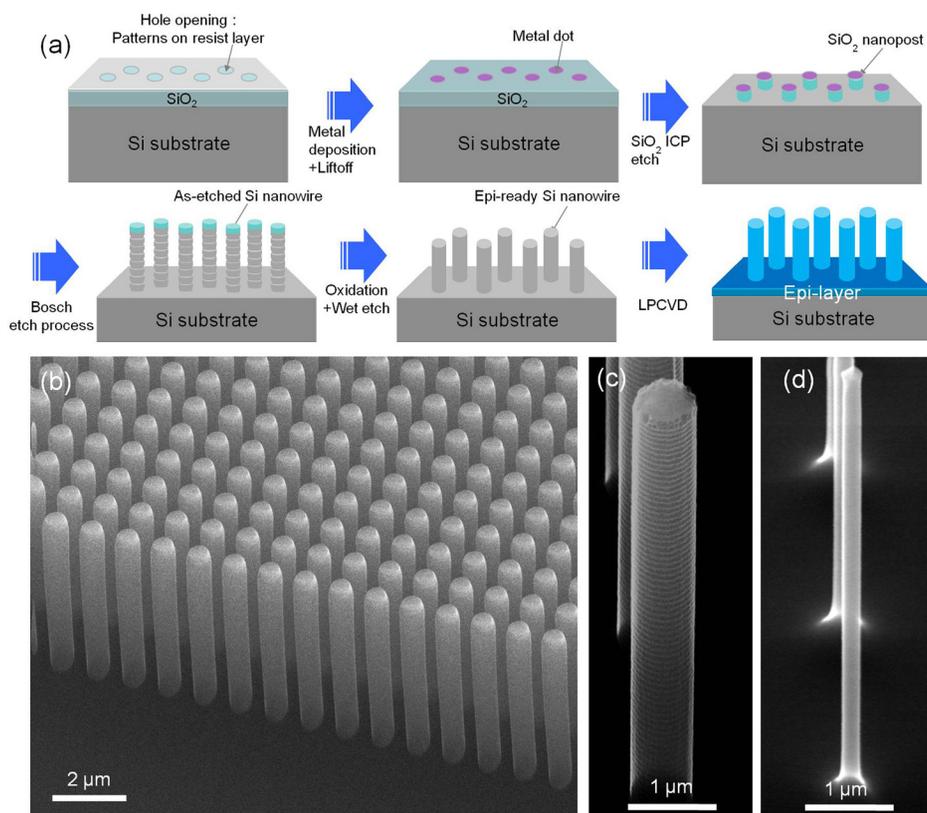


FIG. 1. (a) Schematic of the preparation sequence for radial growth of Si nanowire arrays. (b) An SEM image (45 $^\circ$ view) of a section of an array of $\sim 10^6$ Si nanowires (diameter = 500 nm, length = 7 μm , pitch = 1 μm) after Bosch etching step. (c) Higher magnification SEM of Si nanowire in (b) showing periodic scalloped surface morphology due to Si Bosch process. (d) Same nanowire as in (c) after surface oxidation and dilute HF striping to obtain a smooth surface ready for epitaxial growth; diameter is 210 nm.

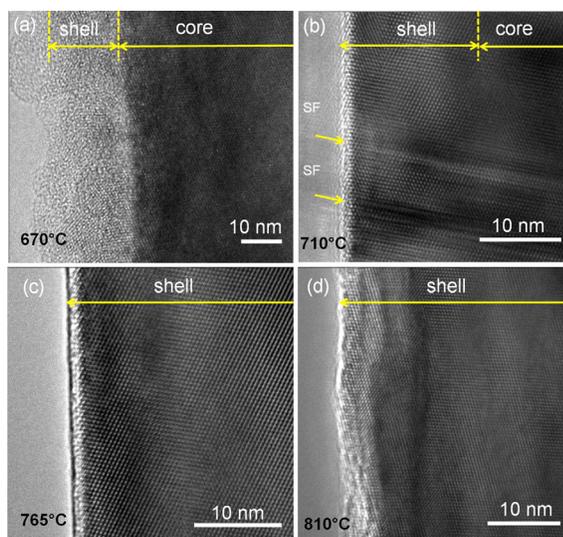


FIG. 2. HRTEM images of undoped Si shells on Si (111) oriented nanowires after radial growth for 3 min at 15 mTorr for growth temperatures and resulting shell thicknesses of (a) 610 °C (10 nm), (b) 710 °C (20 nm), (c) 765 °C (40 nm), and (d) 810 °C (90 nm). The Si shell is fine grain polycrystalline after 670 °C growth (a) and epitaxial single crystal at the higher temperatures (b)–(d). A thin oxide layer is visible on the Si surface.

single crystalline shell grows with occasional stacking fault (SF) defects and for the growth at 710 °C, high quality epitaxial growth resulted with no visible defects observed by TEM. This temperature is much lower than the 950 °C at which defect-free, single crystalline phosphorous doped Si radial shell using SiH_4 and PH_3 was previously reported for radial crystalline growth by atmospheric pressure CVD.¹⁵ Growth of single crystalline Si radial shells at temperatures lower than 900 °C without post annealing provides a useful process to prepare abrupt and well-defined *p-n* junctions with a low concentration of intrinsic autodoping, and it ensures low diffusivities with little migration of dopants ($<10^{-15}$ cm²/s corresponding to <1 nm) at these temperatures.¹⁷ As indicated by the yellow arrows in Figs. 2(a)–2(d), the undoped shell growth rate increases as growth temperature increases. Additionally, Fig. 2(d) may indicate some roughening of the surface of the 90 nm-thick undoped Si shell grown at 810 °C. Thermally activated enhancement of adatom migration and surface reaction rates at higher temperatures results in increased epitaxial growth rates and may result in some increase in surface roughness under certain conditions.

For the controlled formation of radial doped junctions, it is important to understand associated kinetic and thermodynamic factors impacting the growth and morphology—and in turn PV performance—of the undoped and doped Si shells separately prior to growing the composite radially doped structure. The epitaxial shell thickness vs. growth time (see Fig. 3) indicates linear growth kinetics for both doped and undoped radial growth. The growth rate is limited by the precursor mass transport at these mTorr pressures, so that the single crystalline Si radial shell growth rate can be controlled by the SiH_4 partial pressure. In addition, significant reductions in the radial growth rates from that for intrinsic Si epitaxy are observed upon dopant additions for the high doping concentrations used here ($\sim 10^{19}$ /cm³). For intrinsic Si homoepitaxy at 810 °C, the radial epitaxial growth rate is 30.1 ± 2.7 nm/min. In contrast

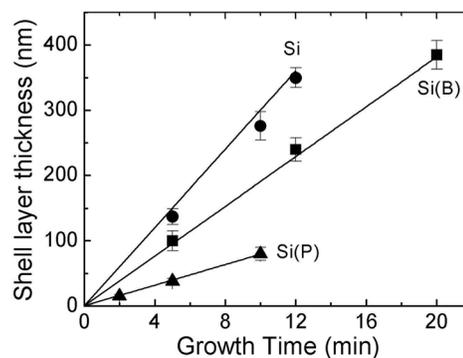


FIG. 3. Shell layer thickness vs. growth time of undoped, B-doped, and P-doped Si radial epitaxial growth at 810 °C on NWs of 500 nm diameter showing decreased growth rates when B and P dopants are present.

heavily B-doped radial growth is observed to decrease to 19.1 ± 1.7 nm/min and for P-doped shell, the radial growth is further reduced to 7.9 ± 1.0 nm/min. In general, CVD planar growth at high B and P concentrations is known to result in reduced Si and SiGe growth rates due to dopant segregation on the surface.^{18–20} For example, P ties up dangling Si bonds and reduces the dissociative adsorption rate of the Si precursors, thereby reducing the growth rate.¹⁹

Thermodynamic and kinetic processes also determine the equilibrium crystal shape and surface growth morphology and can be greatly affected by the presence of impurities, including dopants, on surfaces. In addition, we might expect such effects to be enhanced by the curved surfaces of the NWs due to the presence of a high density of surface steps. Thus, to further elucidate Si epitaxy on the NW surfaces, we examined the effect of dopants on surface morphology. The SEM images of single NWs in Figs. 4(a)–4(c) are shown for intrinsic, *p*-type (B-doped), and *n*-type (P-doped) Si epitaxy at 810 °C for a fixed time of 10 min and correspond to shell thicknesses of 300, 200, and 85 nm, respectively. These results indicate a strong influence of the presence of dopants on surface morphology during Si radial shell growth for these [111] oriented Si NWs. In all cases, side-wall facets develop during epitaxy from the initially smooth, curved surfaces of the NWs. For the greater shell thicknesses of the undoped and B-doped Si radial shells an additional feature, a multi-faceted “match-head” structure, is observed that forms at the tip of the NW.

The crystallographic orientations of sidewalls and match-head structures were investigated by high-resolution transmission microscopy. The sidewalls of the Si radial shells in all cases (undoped, B-doped, and P-doped) consist of the six {110} planes bounding the sides of the [111] oriented NWs. The equilibrium shape of sidewalls and match-head structure is governed by the crystal orientation-dependent growth rate and thermodynamic stability. From a kinetic growth rate perspective, a plane with higher surface free energy (specific surface energy) tends to grow faster in its normal direction than planes with lower surface free energy. As a result, the planes with the lower surface free energy become the dominant planes defining the radial growth sidewalls. In this case for Si [111] NWs, the {110} planes are not favorable to form sidewalls because the surface energy of 1.43 J/m² for the (110) plane is higher than

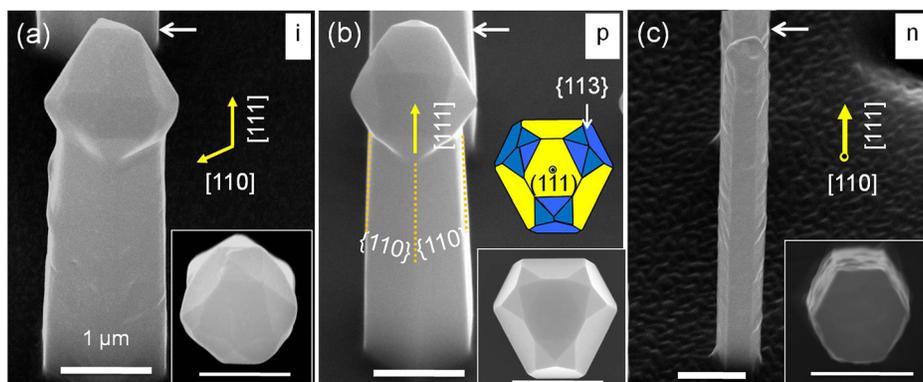


FIG. 4. SEM images (45° view) of Si [111] oriented nanowires after radial epitaxial growth at 810 °C for (a) undoped, (b) B-doped, and (c) P-doped Si shells showing {110} faceted side walls in all cases and for the undoped and B-doped cases, a “match-head” faceted top. The SEM insets are images of the same nanowires taken from a top-view and the colored schematic inset in (b) shows the crystallographic orientation of the facets for the B-doped match-head with yellow corresponding to {111} facets and blue to {113} facets. Yellow dotted lines in (b) demark the edge of the facets. All white bar markers are 1 μm and the white arrows indicate a second Si nanowire in the background.

that of 1.36 J/m² for the (100) plane.²¹ However, {110} and {311} planes are thermodynamically stable as confirmed by thermal annealing studies.²² Additionally, rounding induced by inherent cross-sectional shape of the NW introduces minima of surface energies of {110} and {311} planes and results in significant faceting for these surfaces.²¹

The match-head structure provides additional information on the 3D shape for Si epitaxial growth at small dimensions, because the structure can be nucleated along the circumference of the small diameter NW top surface and proceed to grow in a nearly unconstrained fashion along both lateral and vertical directions. Faceting at the tip of grown Si NWs after subsequent CVD growth at higher temperatures (950 °C) has also been reported.¹⁵ The undoped and B-doped Si match-head facets are shown in Figs. 4(a) and 4(b) in both 45° inclined and top (see insets) views for 810 °C growth. The {111} and {113} crystallographic facets at the Si [111] NW tip are identified by the yellow and blue colors, respectively, in the inset in Fig. 4(b) for the case of the B-doped Si shell growth. The top-region of B-doped Si shell is seen to be composed of a (111) plane at the center and inclined {111} and {113} planes surrounding the (111) plane. A similar set of facets was observed for Si [111] NW after growth of undoped CVD Si shell (Fig. 4(a)). The only observed differences between B-doped and undoped shells are the smoother and more distinct facets for the B-doped case, which may be related to B-induced lowering of the S_A step energy on Si surfaces.²³ For undoped Si, the growth rate of {110} planes is faster than that of {111} planes because the latter have the lowest surface free energy.²¹ Thus, the {111} planes become the dominant facets bounding the three-dimensional equilibrium shape at the NW tip for these vapor-solid growth conditions with the {113} planes that are also seem to be present to complete the tip morphology. In addition to surface energy anisotropy, the presence of dopants on the surface is another factor which may influence the crystal morphology. The {113} faceting shown in Fig. 4(b) is consistent with previous observations of {113} facet formation on (100) Si thin films at high B coverage for growth above 600 °C.¹⁸ In contrast, for P-doped Si radial shell growth, the NW exhibits {110} sidewalls and a (111) top facet with no clear development of {111} or {113} facets around the NW tip, perhaps due in part to the much thinner grown shell

(85 nm) as a result of the P-coverage induced reduction in the Si growth rate.¹⁹ Also, the sidewall surface facets for P-doped Si radial shell growth show much rougher surfaces. This morphology results because P tends to segregate on the surface of Si during growth at high P levels and terminate Si surface dangling bond sites which inhibits uniform surface growth.¹⁹ We note that due to the similarity in surface energies and planar growth behavior of Si and Ge, similar sidewall and match-head morphologies may be anticipated for Ge radial NW growth.

To further access the quality of the present low temperature Si radial epitaxial growth method, large arrays of vertical *p-i-n* NWs were grown and PV devices were fabricated. Epitaxy-ready surfaces of arrays of $\sim 4 \times 10^4$ *p*-type ($3 \times 10^{18} \text{ cm}^{-3}$) Si NWs of 7 μm length and 5 μm pitch were prepared in an area of $1 \times 1 \text{ mm}^2$, and then radial epitaxial growth of *p-i-n* structures was carried out under the same fabrication and growth conditions as has been described above. Starting with initial NW diameters of 1.05 μm , CVD growth of a 60 nm *p*-type shell was followed by a 150 nm *i*-region and then a 90 nm *n*-type shell without interruption for a final diameter of 1.65 μm . These diameters of Si NWs are anticipated to be smaller than minority carrier diffusion lengths based on our earlier scanning photocurrent studies on axial *p-n* junction NWs.²⁴ The NW array was protected by multistep photoresist deposition (AZ4330RS) and then removed after a mesa structure was etched for electrical isolation followed by deposition of a bottom 100 nm Ni contact to the *p*-type substrate and a top Ti/Au contact of thickness 50/100 nm on top of the *n*-doped planar epitaxial growth region along two sides of the array (left inset of Figure 5). Current-voltage (*I-V*) measurements for one of the arrays in the dark and under illumination are shown in Fig. 5, indicating the expected diode behavior. The PV properties of Si radial *p-i-n* junction NW arrays were characterized by *I-V* measurements under Air Mass (AM) 1.5G illumination. To preclude the contribution from the planar regions outside radial *p-i-n* junction NW arrays, all areas except the radial *p-i-n* junction NW arrays were screened with black paper. Measurements in a solar simulator under AM 1.5G illumination gave an efficiency of 10%, with a short circuit current density of 40 mA/cm², an open circuit voltage of 0.44 V, and a fill factor (FF) of 0.38. These radial *p-i-n* NW array results

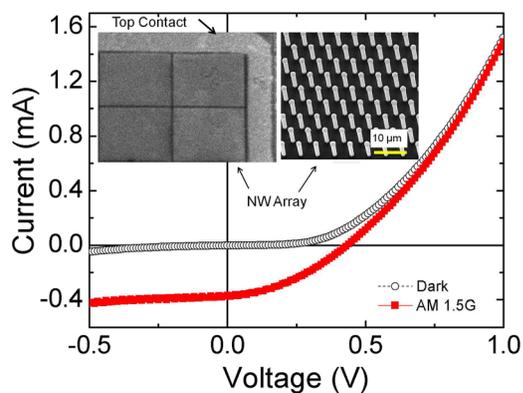


FIG. 5. Electrical I - V response of Si $\langle 111 \rangle$ radial p - i - n nanowire array measured at AM 1.5 G illumination indicating a $V_{OC} = 0.44$ V, $J_{SC} = 40$ mA/cm², FF = 0.38, and efficiency = 10%. Insets show an SEM at 45° of NW array (right side) and a lower magnification optical micrograph of the 4 segment ~ 1 mm² nanowire array with Ti/Au top contacts above and to right of the array (left side).

compare favorably to the previous highest reported efficiency of 10.8% for PV devices based on arrays of ion implanted Si radial p - n junctions.³ The results are particularly promising since the present arrays are based on relatively large NW-to-NW spacings desired for the current growth studies, whereas the previous studies, which used ion implantation to form the radial junctions, employed smaller spacings and top-down etching to achieve a more optimized tapered cone-like NW shape (170–400 nm diameter).³ Also, studies of Si MW arrays with much larger diameters (7.5 μ m) and lengths (25 μ m) fabricated by top-down etching and dopant diffusion reported slightly lower efficiencies of 8.7% and current densities of 20 mA/cm².⁵

The present 10% efficiency for our radial p - i - n NW arrays also can be compared to previous single wire PV studies. For example, the highest efficiency reported for a single 1.2–1.8 μ m-diameter and 25 μ m-long Si MW prepared by Cu catalyzed growth, P diffusion, and surface passivation with amorphous hydrogenated SiN layer was 9%.⁶ For a single 200 nm-diameter Si NW with back-side reflector prepared by a bottom-up and epitaxial shell growth approach, efficiencies of 5.9% were achieved.¹⁶ Thus, compared to previous array and single wire radial junction studies, the present 10% PV efficiency obtained from 7 μ m-long and 1.65 μ m-diameter non-optimized Si radial p - i - n junction arrays with relatively large pitch suggests that single crystalline Si radial shell growth with well-controlled dopant profiles and interfaces provides significant opportunities for further enhancing PV efficiency of Si radial p - i - n junction devices.

In summary, single crystalline doped and undoped Si radial shell growth at low temperatures on vertical Si nanowire arrays has been demonstrated by low pressure chemical vapor deposition. Temperature- and time-dependent studies of Si homoepitaxy on nanowire surfaces have provided fundamental understanding of growth kinetics and faceting for Si radial shell growth. Multiple faceting at the top of the Si nanowires results in a match-head type structure due to surface energy anisotropy for intrinsic and B-doped growth. These fundamental studies of Si radial shell growth give useful guidelines on the formation of Si radial p - n and p - i - n junctions for photovoltaic cell device applications. Based on

our radial growth method, excellent power conversion efficiencies for Air Mass 1.5 Global solar illumination of 10% and short circuit current densities of 40 mA/cm² are demonstrated for non-optimized architectures.

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