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Ultrashort Channel Silicon Nanowire Transistors with Nickel Silicide Source/Drain Contacts

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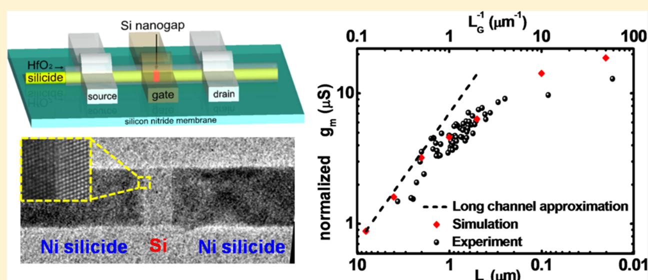
S Supporting Information

ABSTRACT: We demonstrate the shortest transistor channel length (17 nm) fabricated on a vapor−liquid−solid (VLS) grown silicon nanowire (NW) by a controlled reaction with Ni leads on an in situ transmission electron microscope (TEM) heating stage at a moderate temperature of 400 °C. $NiSi_2$ is the leading phase, and the silicide−silicon interface is an atomically sharp type-A interface. At such channel lengths, high maximum on-currents of 890 (μA/μm) and a maximum transconductance of 430 (μS/μm) were obtained, which pushes forward the performance of bottom-up Si NW Schottky barrier field-effect transistors (SB-FETs). Through accurate control over the silicidation reaction, we provide a systematic study of channel length dependent carrier transport in a large number of SB-FETs with channel lengths in the range of 17 nm to 3.6 μm. Our device results corroborate with our transport simulations and reveal a characteristic type of short channel effects in SB-FETs, both in on- and off-state, which is different from that in conventional MOSFETs, and that limits transport parameter extraction from SB-FETs using conventional field-effect transconductance measurements.



KEYWORDS: *Nickel silicide, silicon nanowire, short channel, Schottky barrier field effect transistor, in situ TEM*

Vapor−liquid−solid (VLS) grown semiconductor nanowires (NWs) have been intensively investigated as candidates of electronic devices due to their decent crystal quality,[1] easiness of control over the lateral confining dimension,[2,3] and potential for bottom-up self-assembled circuits.[4−6] Field-effect transistors (FETs) built on VLS grown Si, Ge, and SiGe heterostructure NWs have shown high carrier motilities and excellent transistor characteristics comparable to or better than those fabricated by top-down processing approaches.[7,8] One of the primary motives for these investigations is the fact that their gates can be formed in a Ω-gate or gate-all-around geometries and have therefore superior electrostatic coupling between gate and channel over other device architectures.[9] However, enhanced FET performance is enabled with ever-smaller channel lengths that can provide high on-current drives. The NW transistor channel length is usually defined by the metal gate width or the distance between its source/drain (S/D) electrodes, both of which are limited by lithography patterning tools. With continual transistor down-scaling, the demands on the critical dimension (CD) control in lithography tools steadily increases. For CD below 20 nm, very expensive e-beam lithography tools or sophisticated photo-lithography technologies (extreme ultraviolet source, double patterning, etc.) are needed.[10]

By extending earlier works[11,12] on controlled silicide formation in in situ TEM experiments, we developed a process that can overcome the resolution limit posed by lithography technologies in defining transistor channels. Using this technique, we demonstrate SB-FETs with ultrashort channel lengths down to 17 nm on VLS grown Si NWs. Compared with the conventional MOSFET, a SBFET has naturally abrupt junctions and is not limited by lateral doping profiles, which are determined by the doping/activation techniques[13,14] and become increasingly difficult for ultrashort channel devices. Our investigation also includes the silicidation reaction fundamentals (phase formation and growth kinetics), which is important to achieve a fine control over transistor channel lengths previously not achieved with VLS NW FETs. The controlled channel formation using this technique enabled us to access a new domain of SB-FET operation and to identify a performance transition between long channel and short channel regions in SB-FETs with an overall transport performance that is in excellent agreement with our transport simulations. Further, our systematic transport studies elucidates the essential

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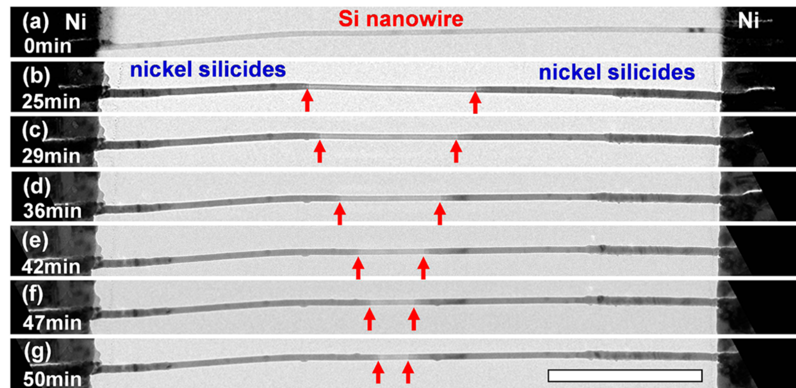

Figure 1. (a−g) Series of in situ TEM snapshots showing the growth of nickel silicide from S/D Ni electrodes and narrowing of the middle silicon segment. The red arrows indicate the silicide/silicon reaction front. The scale bar is 1 μm.

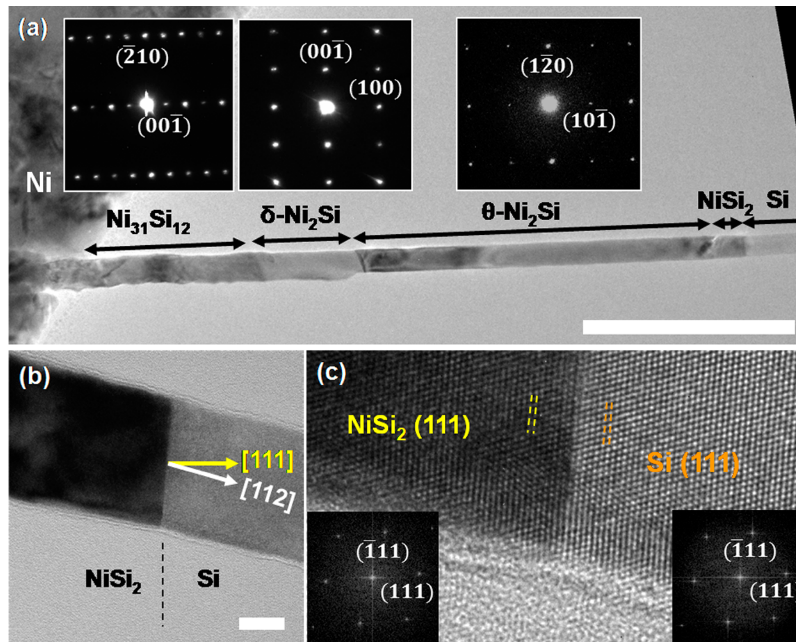

Figure 2. (a) TEM image with selected diffraction patterns that determine the nickel silicide phase sequence: Between Ni and Si, several phases are formed including $Ni_{31}Si_{12}$, δ-Ni_2Si, θ-Ni_2Si, and $NiSi_2$. Zone axes for inset diffraction patterns from left to right are [120], [010], and [212], respectively. The scale bar is 400 nm. (b) Zoom-in TEM image of the $NiSi_2$/Si interface, showing that the reaction front is the Si (111) plane even in a ⟨112⟩ grown silicon NW. The scale bar is 20 nm. (c) HRTEM image of the atomically flat $NiSi_2$/Si interface. The crystal orientation across the interface corresponds to a type A interface. The epitaxial relationship is established as $NiSi_2$ (111)//Si (111) and $NiSi_2$ $[\bar{1}10]$//Si $[\bar{1}10]$.

role of Schottky barriers in charge transport in ultrashort channel FETs and demonstrate that transport parameter extraction using conventional transconductance methods from SB-FETs may not be accurate. The implications of this analysis can be generalized to other NW SB-FETs.

Material Considerations in Nanochannel Silicidation. Nickel silicides are the standard metal contacts used in the semiconductor industry for both NMOS and PMOS devices and are regarded as "midgap" metals with a hole Schottky barrier height (SBH) of ~0.4 eV.[15,16] Moreover, nickel silicides (or their counterparts, nickel germanides in germanium devices) have been extensively explored as nanoscale contacts for semiconductor NWs[17−21] and therefore our choice as the electrical contacts to Si NW devices. In the Ni−Si reaction, Ni is the dominant diffusing species (DDS), and multiple nickel silicide phases could form.[22] Different nickel silicide phases have different Ni solubility and diffusivity,[23] and the growth of a more Ni-rich phase by consuming a less Ni-rich phase also needs Ni supplies from the metal contact reservoir. The phenomenon of simultaneous growth of multiple phases complicates the kinetics analysis that uses the data of silicided segment length versus time. To better understand and control the Ni−Si reaction kinetics for the fabrication of ultrashort channel FETs, we examine first the nickel silicide phases in our silicided NW segments and provide a detailed analysis on the silicide−silicon interface structure and quality that can have direct impact on formed silicide/silicon barrier heights and charge injection.

Our SB-FET devices were fabricated on 50 nm thick silicon nitride TEM membranes with a window size of 250 μm × 250 μm. Source/drain Ni contacts were defined by photolithography, followed by 100 nm e-beam evaporated Ni layer. The native oxide on the Si NWs at contact openings is removed before metallization. After S/D metallization and to avoid creation of defects in the native oxide layer on the Si channel during the subsequent high energy electron radiation (300

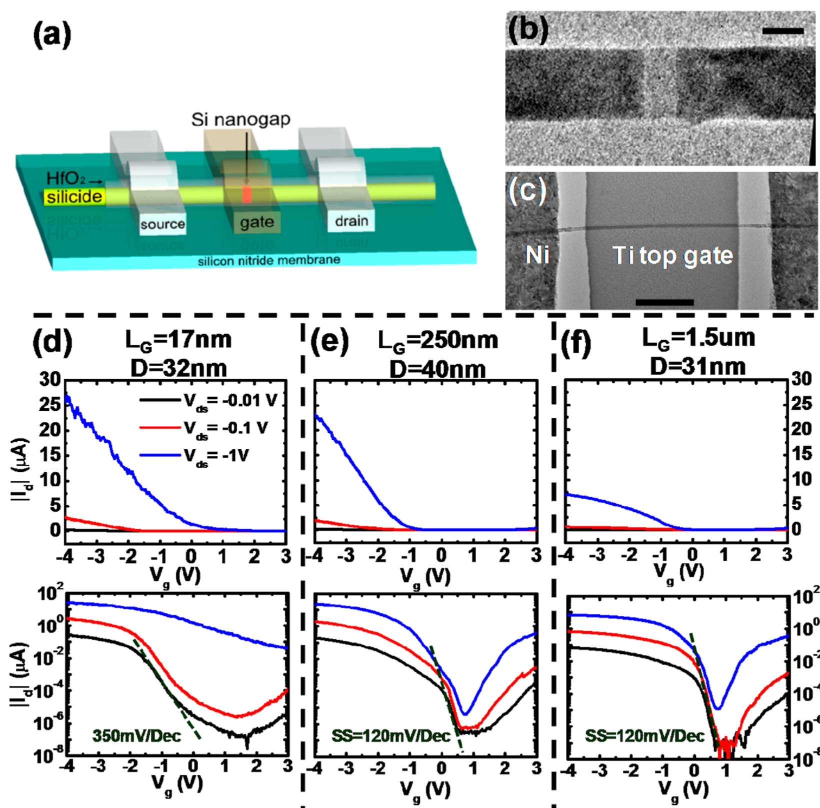

Figure 3. (a) Schematics of the top-gate FET device with ultrashort silicon channel (Si nanogap). (b) TEM image of a 17 nm silicon channel. The scale bar is 20 nm. (c) TEM bright field image of a top gate Si NW SB-FET fabricated on silicon nitride membrane. Scale bar is 1 μm. (d−f) Transfer curves with both linear (top panels) and log (bottom panels) for devices with channel lengths of 17 nm, 250 nm, and 1.5 μm and diameters of 32 nm, 40 nm, and 31 nm, respectively. The V_{ds} in each plot from low to high are −0.01 V (black), −0.1 V (red), and −1 V (blue).

keV) in TEM (Tecnai F30), we went through a special procedure[24] to remove this native oxide layer.

Annealing of the sample was performed on an in situ TEM heating stage (Gatan 628 single tilt heating holder) at 425 °C, and the reaction was monitored in real time. Initially, nickel silicide formed at the source/drain Ni/Si contact and grew inward by transforming Si NWs. The remaining Si segment of the NW shrinks as the reaction proceeds. Figure 1a−g shows a series of TEM snapshots during the reaction process. If not interrupted, the whole Si NW would be fully converted into a metallic nickel silicide NW. However, we are interested in using this process to demonstrate that we can dynamically control the length of Si segment and use it as the channel in FET devices. When the length of the Si segment (referred as Si channel thereafter) reaches a desired length, we stop heating the sample, which thereafter cools down quickly (~10 °C/s), and the interface is frozen. To fabricate an ultrashort Si channel, very precise control of the reaction process or the silicide growth rate is required. In the final stage of Si channel length tuning, the silicide growth rate was reduced to about 0.05 nm/s at 375 °C, which allows for sub-nanometer fine control over the channel length.

We find that there are multiple phases formed on the Si NW as the reaction front swept through (Figure 2a). The phases are determined by electron diffraction patterns and fast Fourier transformation (FFT) of high resolution (HR) TEM images obtained from at least two different zone axes. The leading phase in direct contact with Si is $NiSi_2$, which is immediately followed by θ-Ni_2Si within a distance of 50 nm. Going further outward in the direction to the Ni leads, the θ-Ni_2Si is followed by a δ-Ni_2Si segment. Then, a more nickel-rich phase $Ni_{31}Si_{12}$ follows in direct vicinity with the Ni leads. During the process of silicidation, Ni is added into the Si crystal, and the resulting Ni−Si compound volume is generally greater than the original Si volume, which appears as a diameter expansion compared with the as-grown Si NW diameter (Figure 2a). The only exception of volume expansion resides in the $NiSi_2$ phase because of its close similarity in crystal structure with Si. We observe diameter expansion when Si is transformed to θ-Ni_2Si, δ-Ni_2Si, or $Ni_{31}Si_{12}$. This phase sequence is in contrast with the results obtained in a thin film reaction between planar Si and Ni thin films, which were established from in situ XRD and resistance measurements during the temperature ramp up.[25] In thin film studies, δ-Ni_2Si is the first phase formed at a temperature as low as 200 °C, transformed to NiSi as the temperature is raised above 350 °C, and finally converts to $NiSi_2$ at above 750 °C.[26] The expected NiSi phase was not observed in our experiments, which corroborates with earlier results from the reaction between Ni pads and Si NWs at 550 °C,[27] 450 °C,[28] and 360 °C,[29] and from the reaction between Ni thin films and Si wafers at 450 °C,[30,31] all of which showed $NiSi_2$ as the leading phase at temperatures well below 750 °C. It has been suggested that the interfacial oxygen may play a role in mediating $NiSi_2$ formation at low temperature;[31] however, there is currently no definite explanation of the mechanism of low temperature formation of $NiSi_2$. Another silicide phase θ-Ni_2Si, which follows $NiSi_2$ in the upstream direction toward the Ni leads, has a hexagonal lattice structure (a = 3.836 Å, b = 4.948 Å). According to Ni/Si phase diagram, θ-Ni_2Si is a high temperature phase, which is stable above 825 °C. However,

recent studies on Ni and Si NW reaction have also found θ-Ni_2Si formed at a low temperature.[32] Moreover, in situ X-ray diffraction studies of Ni−Si reaction shows that θ-Ni_2Si is a transient phase, which appears first at low temperatures but disappears as the temperature is increased.[33] This is in good agreement with our results in that θ-Ni_2Si is also quickly consumed by δ-Ni_2Si after it forms. Another experiment[34] to test the stability of this phase shows that the θ-Ni_2Si phase formed at high temperatures transforms into δ-Ni_2Si and ε-Ni_3Si_2 as predicted by the phase diagram as it is cooled down below its stable temperature, 825 °C. On the other hand, θ-Ni_2Si formed at a low temperature (460 °C) does not decompose during temperature cool down even to room temperature. These experiments suggest that, although θ-Ni_2Si is a high temperature phase, it has a certain type of stability at low temperatures, likely due to high kinetic barriers for phase transformation.

Among all of the phases and interfaces formed along the NW axial direction, the $NiSi_2$/Si interface is the metal−semiconductor contact interface. It is interesting to observe that the Ni−Si reaction front is an Si (111) plane, even in a ⟨112⟩ grown Si NW (Figure 2b,c). The high resolution transmission electron microscopy (HRTEM) image in Figure 2c shows that the interface is atomically sharp, and the epitaxial relationship established from the image is $NiSi_2$ (111)//Si (111) and $NiSi_2$ $[\bar{1}10]$//Si $[\bar{1}10]$. The slanted interface observed here has a larger area compared with a cross-sectional plane that is perpendicular to the NW growth direction. The fact that the silicide−silicon NW system chooses to form a larger interfacial area implies that the Si(111)/$NiSi_2$(111) interface has lower energy than that of all other possible interface configurations. In a reaction between Ni thin film and Si (001) wafer, inverted $NiSi_2$ pyramids[31,35,36] with {111} facets form inside the Si wafer, showing the same reaction front as we observe here. It is known that the $NiSi_2$/Si interface is among the best quality metal semiconductor interfaces,[37] because the two crystals share the same cubic structure and a very close lattice constant (a_{Si} = 5.430 Å, a_{NiSi_2} = 5.406 Å). The interfacial electronic properties are determined by the detailed structure of the $NiSi_2$/Si interface. Two types of $NiSi_2$/Si interfaces can form with a difference in their crystal orientations across the interface. $NiSi_2$ has the same orientation with Si in a type-A interface, while it is rotated 180° about the interface normal axis with respect to Si in a type-B interface. It is known[38] that these two interfaces have different SBH with *n*-Si (0.65 eV on type-A and 0.78 eV on type-B). In a large area thin film reaction,[36] usually the $NiSi_2$/Si interface is a mixture of type-A and type-B. In contrast, throughout the HRTEM characterization of our nanoscale contacts, we consistently observe atomically sharp type-A $NiSi_2$/Si interface, which guarantees the reproducibility of the electronic properties of the metal−semiconductor contact.

Device Analysis of Ultrashort Channel SB-FETs. With this thorough understanding of formation, structure, and expected electronic properties of our silicide-Si NW interface, we are able to precisely scale down the channel length of a $NiSi_2$−Si NW transistor and explain its carrier transport characteristics. The silicide growth rate can be controlled by carefully tuning the temperature at the final stage of the silicidation reaction. The schematic of our top-gated Si FET device structure is shown in Figure 3a, with an ultrashort channel (Si nanogaps) highlighted on the Si NW. We have obtained a 17 nm Si channel on a VLS grown Si NW (Figure 3b) at a temperature of 375 °C. HfO_2 gate dielectric (10 nm) was conformally deposited on the Si NW devices using atomic layer deposition at 200 °C. At this temperature, no further silicidation was observed, and the Si channel length was retained at the desired value. Finally, 100 nm Ti was deposited as the top-gate electrode. Figure 3c shows a TEM bright field image of the fabricated device on the 17 nm Si NW channel (Figure 3b). $NiSi_2$ is still the leading phase in such very short Si NW channels (Figure S2, Supporting Information (SI)). In our devices, the leakage current from gate electrode to S/D nickel silicide extensions is small (<1 pA when $V_g = -4$ V), and we are only interested in DC characteristics of the device, so the gate-S/D overlapping was not of concern. To better gauge the characteristics of the Si FET with an ultrashort channel, we have also fabricated devices with longer Si channels with the same gate dielectric layer. As suggested in ref 39, we perform a postmetal-gate annealing step for 60 s in forming gas at 300 °C to passivate the interface traps at the Si/HfO_2 interface. This treatment step consistently improves the gate control on the channel so that both the on-current and inverse subthreshold slope (SS^{-1}) were substantially improved (see the SI, Figure S5 for a comparison).

Transfer curves (both in linear scale and log scale) of Si NW FET with channel lengths, L_G = 17 nm, 250 nm, and 1.5 μm are shown in Figure 3d−f. As the transistor channel length is scaled down, the on-current I_{on} at $V_{ds} = -1$ V increases from 7 uA (L_G = 1.5 μm) to 23 uA (L_G = 250 nm) and finally to 27 uA (L_G = 17 nm). This trend is intuitively expected, since we are measuring current from a shorter Si segment at the same bias; this trend however does not scale linearly as we will discuss below. The series resistance of the nickel silicide S/D extension can be neglected even in our shortest channel devices, based on electrical measurement of a fully silicided Si NW of the same length as well as calculation of the resistance using known resistivity values of nickel silicides from literature (see Table S1 and Figure S3 in the SI for more details).

The increase in on-current is desirable because it allows faster operation of logic circuits (or lower power consumption if the current is held constant at a reduced supply voltage). On the other hand, the SS^{-1} degrades from 120 mV/Dec for L_G = 250 nm channel device to 350 mV/Dec for L_G = 17 nm ultrascaled channel device. The off-state leakage current also increases in the 17 nm device. The I_{off} and SS^{-1} degradation are attributed to insufficient gate control over the NW channel electrostatics in such devices with close proximity of S/D when switching the device off. We note here that our NW has a diameter of 30 nm. Both SS^{-1} and I_{off} are expected to be improved if a thinner NW (thin body) was used.

Higher on-state conduction is one of the motivations that drive the semiconductor industry to devote increasing endeavors in down-scaling of the MOSFET channels. To assess the on-state performance as a function of channel length, we use the maximum transconductance g_m ($V_{ds} = -1$ V) as a figure-of-merit and compare experimentally extracted values from 64 devices with those obtained from transport simulations. In a long channel approximation, g_m is inversely proportional to L_G and is given by

$$g_m = \frac{\mu_h V_d C_G}{L_G^{\ 2}} \qquad (1)$$

where g_m is the maximum transconductance of an individual device, μ_h is the hole mobility, L_G is the channel length, V_d is the drain bias, and C_G is the gate capacitance. To correlate the geometrical factors of the gate capacitance, we developed an empirical formula for Ω-gate capacitance, C_G^{Ω}, by curve fitting to capacitance values obtained from finite element simulations,

$$C_G^{\Omega}(h, r) = L_G\left[2\pi - 2\arccos\left(\frac{1 - h/r}{1 + h/r}\right) + a(h/r) + b(h/r)^2\right]\varepsilon_0\varepsilon_r/\ln[1 + h/r] \quad (2)$$

Here, r is the radius of the NW, h is the dielectric layer thickness, and ε_r is the relative dielectric constant of the gate insulator layer. In a top-gated NW FET, the gate covers a portion of the surface of the NW. The term $2\arccos((1 - h/r)/(1 + h/r))$ accounts for the central angle of the uncovered circular sector of the NW cross-section by the gate metal. $a(h/r)$ and $b(h/r)^2$ are first- and second-order correction terms of the tangential fringing fields. Equation 2 reduces to the well-known cylindrical capacitance $C_G(h,r) = 2\pi L_G\varepsilon_0\varepsilon_r/\ln[1 + h/r]$ with a fully surrounded gate (first two terms in braces of eq 2 = 2π) and in the absence of asymmetric fringing fields ($a = b = 0$). For the case of thin dielectrics in a Ω-gate configuration ($h/r < 1$), the fringing field parameters were found to be $a = 2.086$ and $b = 0.852$ which yields capacitance values that are within 2% error of those obtained from 2D simulations. In the extreme of $h/r \ll 1$, the gate capacitance can be approximated by a parallel plate capacitor with curved surfaces, and therefore the tangential fringing fields can be neglected. In the simulation, we found that the gate capacitance increases by only 2.6% when the substrate dielectric constant increases from 3.9 to 22, which implies that the substrate (nitride TEM membrane) stray capacitance is not important. The axial fringing fields may affect the gate capacitance when the channel is very short (or S/D electrodes are very close). However, the change of capacitance per unit length due to axial fringing fields is less than 3% even when the channel length shrinks down to 15 nm (Figure S4, SI). Therefore, our comprehensive simulations ensure a wide applicability of eq 2. To compare different devices whose diameters vary in the range of 30−50 nm, we normalize our experimental transconductances with respect to the gate capacitance of a virtual reference device (40 nm in diameter, top gate device with 10 nm HfO_2 gate dielectric) using the formula:

$$g_m^{\text{normalized}} = g_m \frac{C_G^{\text{ref}}}{C_G} \quad (3)$$

where $C_G^{\text{ref}} = C_G^{\Omega}$ (h = 20 nm, r = 20 nm), and $C_G = C_G^{\Omega}(h,r)$.

To validate the on-state characteristic trend observed in the experimental devices, we have performed device simulations for the same experimental channel length range using the Silvaco Atlas software package. The transport model for Schottky contact is essential in this simulation, and it implements the model described in ref 40, which treats the tunneling current through the Schottky barrier as carrier generation and recombination process in the barrier region, and the model can be extended for sub-50 nm channels. A diffusion-drift model along with energy balance equations, which account for hot carrier effects, was solved for both carriers. The mobility model is taken after ref 41, which accounts for velocity saturation at high parallel fields (along channel length), and surface roughness scattering as a function of perpendicular field, which was calibrated against the Si universal mobility curve. We assumed a gate-all-around geometry for gate capacitance in the simulation, and $C_G = ((2\pi\varepsilon_r\varepsilon_0)/(\ln(1 + h/r))$ was used in eq 3 to normalize simulated devices to the reference device. The normalized maximum transconductance $g_m^{\text{normalized}}$ as a function of channel length for both measured and simulated devices is plotted in Figure 4a. Each black circle represents a $g_m^{\text{normalized}}$ for a single experimental device (in total 64 devices with different channel lengths), and the red diamonds are data points extracted from simulations. The trend predicted by the long channel approximation (eq 1) using $C_G^{\text{ref}} = C_G^{\Omega}$ (h = 20 nm, r = 20 nm) is represented by a dashed line in Figure 4a. Both of the experimental and simulated devices show deviation from the predicted enhancement of $g_m^{\text{normalized}}$ according to eq 1, with shorter channel lengths. While this deviation is expected in conventional short channel FET devices (e.g., due to S/D series resistance), it manifests itself in a different and more significant physical behavior in SB-FETs.

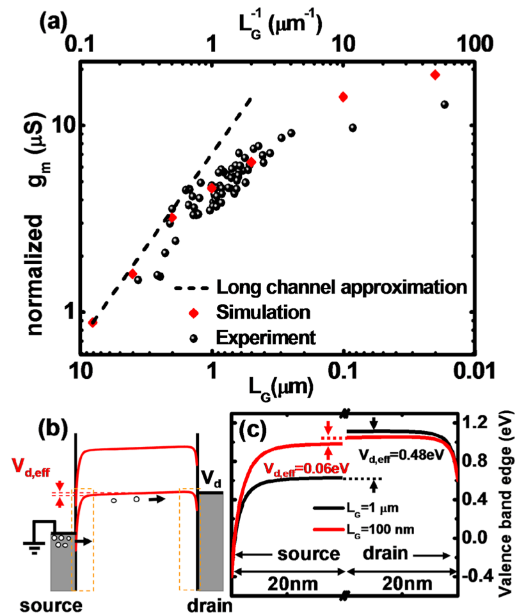

Figure 4. (a) Double log plot of normalized maximum transconductance as a function of channel length. Each black small circle represents the measured transconductance from an individual experimental device, and large red diamonds represent extracted transconductance from simulated devices with different channel lengths. The dashed line describes the trend predicted by the long channel approximation from eq 1. (b) Axial band diagram near the surface of a 100 nm channel device in the on-state. The valence band profile can be divided into three regions (from left to right): the source SB region, channel region, and drain SB region. Both of the SB regions are highlighted by dashed boxes. The voltage drop across the channel region is denoted as $V_{d,eff}$. (c) Comparison of the valence band profile at the source/drain SB region (i.e., the part of the device highlighted by dashed boxes in b) of devices with 100 nm and 1 μm channel lengths during on-state operation ($V_{ds} = -1$ V, $V_g = -4$ V). $V_{d,eff}$ in the 100 nm channel length device is a small fraction of the total source/drain bias.

To explain the origin of maximum transconductance deviation from long channel approximation in SB-FETs, we plot the energy band-edge diagrams along the NW axis in Figure 4b, extracted near the surface of devices under an on-state bias. In Figure 4b, we divide the NW along the axial

direction into three regions: the source SB region, channel region, and drain SB region, where the valence band part of the S/D SB regions are highlighted by dashed boxes. For these undoped NWs, the channel region is the part of the device where the potential drops almost linearly (in a band diagram, the potential drop manifests in the way of band energy increase). This potential drop is defined as effective voltage drop (denoted as $V_{d,eff}$) across the channel, which maintains the channel field to drive carriers but is reduced to only a fraction of total S/D bias V_{ds}. Quantitatively, we plot in Figure 4c the valence band energy profile for devices with different channel lengths (1 μm and 100 nm) along the first 20 nm from both S/D SB regions at $V_{ds} = -1$ V and $V_g = -4$ V (on-state). The $V_{d,eff}$ for $L_G = 1$ μm and 100 nm are 0.48 V and 0.06 V, respectively, with the latter only 6% of the applied V_{ds}. In contrast to the channel region, the majority of V_{ds} drops across the source SB for the short channel device, which implies that the contact resistance at the source is dominant in such a device. This is due to the fact that the source Schottky junction is under reverse bias. In the 100 nm channel device, only a small portion of the voltage drops across the channel, while most of the voltage drops in the S/D SB region, which leads to a thinner SB compared to that of the 1 μm channel device.

The existence of both source and drain SBs poses a limiting factor on the on-current gain from scaled SB FETs. While the thickness of the SB might be controlled by doping, our transport simulations showed that I_{on} or g_m can only be slightly improved at doping densities $>10^{18}$ cm^{-3}, whereas the subthreshold characteristics would be degraded (see SI, Figure S6a). In the on-state ($V_{ds} = -1$ V, $V_g = -4$ V), the SB depletion region thickness for the three doping concentrations considered here (10^{16}, 10^{18}, and 5×10^{18} cm^{-3}) remains essentially the same, about 7 nm (see SI, Figure S6b). This indicates that an increase in doping would not be effective in thinning the SBs to enhance I_{on}. On the other hand, increased channel doping is adverse in terms of incurring carrier scattering and difficulty in turning off the device (e.g., Figure S6a, SI, 5×10^{18} cm^{-3} curve). There are generally other challenges associated with doping in ultrashort FET devices. One of these include random dopant fluctuation, which in the case of our 17 nm device would cause large device-to-device variation including threshold voltage shift, given that only 12 individual dopant atoms should exist in the channel at a doping level of 10^{18} cm^{-3}. On the other hand, the presence of a reservoir effect[42] in the liquid mediating growth seeds in VLS growth prevents realizing complex and sharp doping profiles. The difficulty to scale down the SB thickness becomes an issue in very short channel NW SB-FETs, which are the most common form of NW or nanotube FET devices.[43,44] One possible solution is to utilize the "snow plow" effect that piles up dopants at the silicide−silicon reaction front as the interface moves, to create a highly doped region only close to the contact[45,46] while keeping the channel undoped for better transport characteristics and gate electrostatic control. However, this requires careful optimization of the silicidation temperature and the growth rate to maximize dopant solubility differences in silicon and in the silicide and maintaining high dopant diffusivity in the silicide, which is yet to be accomplished.

With this comprehensive understanding on potential drops across SB-FET devices, we can now note that the use of eq 1 or its similar forms to extract field-effect mobility from top-gate NW transistors is applicable only if the SBH is low[7,8,47] or if the channel is long, when almost all of V_{ds} drops across the channel. If eq 1 is applied to short channel devices (<1 μm) with a moderate SBH, for example, 0.47 eV for holes in our case, the field-effect mobility will be underestimated.[48] For an accurate mobility extraction, one needs to replace L_g and V_d with their effective values ($L_{g,eff}$ and $V_{d,eff}$) in eq 1,[49] where $L_{g,eff}$ is the length of channel region (the silicon segment excluding S/D SB region). Although the boundary of SB region may not be well-defined, the factor $V_{d,eff}$ /$L_{g,eff}$ in eq 1 is well-defined as the average electric field in the channel, which is insensitive to the choice of SB region boundary.

Conclusions. This work presents an investigation of VLS Si NW transistors with a channel length down to 17 nm, by utilizing controlled nickel silicide formation on an in situ TEM heating stage. Multiple nickel silicide phases grow simultaneously with $NiSi_2$ as the reaction front. The $NiSi_2$/Si metal-semiconductor contacts are type-A interfaces, atomically sharp, and therefore have reproducible electronic properties. By combining measured and simulated devices with different channel lengths, our transport analysis shows that the SBs take up the majority of the applied S/D bias when the channel length is scaled down to sub-100 nm region, and the on-state performance deviates from the trend predicted by long channel approximation. This result implies that the Schottky barrier contact engineering is vital to best fulfill performance gains in short channel SB-FETs. In addition, analysis that follows long channel approximation may underestimate the field effect mobility in short channel SB-FETs.

■ ASSOCIATED CONTENT

Supporting Information

Details on native oxide etching prior to silicidation experiments, HRTEM analysis on a 12 nm ultra-short channel device, evaluation of the silicide series resistance from known silicide values and from our experiment, comparison on full 3D simulations and 2D simulations for the Ω-gate capacitance, as well as effects of postmetal gate annealing on device characteristics, and simulated transfer curves for devices with various channel doping levels and their correspondent band-edge diagrams. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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