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An Analytical Model for Dual Gate Piezoelectrically Sensitive ZnO Thin Film Transistors

*Hongseok Oh and Shadi A. Dayeh**

Highly sensitive force sensors of piezoelectric zinc oxide (ZnO) dual-gate thin film transistors (TFTs) are reported together with an analytical model that elucidates the physical origins of their response. The dual-gate TFTs are fabricated on a polyimide substrate and exhibited a field effect mobility of ≈5 $cm^2 V^{-1} s^{-1}$, I_{max}/I_{min} ratio of 10^7, and a subthreshold slope of 700 mV dec^{-1}, and demonstrated static and transient current changes under external forces with varying amplitude and polarity in different gate bias regimes. To understand the current modulation of the dual-gate TFT with independently biased top and bottom gates, an analytical model is developed. The model includes accumulation channels at both surfaces and a bulk channel within the film and accounts for the force-induced piezoelectric charge density. The microscopic piezoelectric response that modulates the energy-band edges and correspondent current–voltage characteristics are accurately portrayed by this model. Finally, the field-tunable force response in single TFT is demonstrated as a function of independent bias for the top and bottom gates with a force response range from −0.29 to 22.7 nA mN^{-1}. This work utilizes intuitive analytical models to shed light on the correlation between the material properties with the force response in piezoelectric TFTs.

1. Introduction

Metal oxides have been widely used for sensing applications[1–3] and their versatile material properties have enabled new functionalities.[4] For electromechanical sensors, the recent development of zinc oxide (ZnO) piezoelectric thin film transistors (TFTs) has paved the way to fabricate high-density force sensor arrays that utilize the TFT as both, a switch and a force sensor.[5–7] In this configuration, the gate electrode switches the TFT and sets its current, and this current can in turn be modulated by external forces that induce changes to the piezoelectric charge density in the TFT channel. This dual functionality enables building active-matrix force sensor arrays with a simple one transistor per cell (1T) structure, combining the performance merit of the active-matrix structure with the merit of a cost-effective simple device architecture. The piezoelectric material must be grown such that the applied forces are normal to its polar crystal surface that exhibits the maximal piezoelectric response, the *c*-axis. Recent research has demonstrated the proposed advantages, such as the ultra-high spatiotemporal resolution in shear force sensation, and its application in closed-loop robotics, in state-of-the-art force sensor arrays.[7]

Despite the successful demonstrations of active piezoelectric devices in force sensor applications, their responsivity has been only qualitatively described by modulation of the energy band-edge profiles.[8] The lack of an analytical model hinders the quantitative prediction of piezoelectric device response to external forces. Recently, we developed analytical models to describe the current response to external forces for active piezoelectric sensors including Schottky diodes and single-gated piezoelectric TFTs as part of a review on piezoelectric semiconductor devices.[9] However, dual-gate TFTs are essential for ZnO films to curb the effects of surface, interface, and bulk traps and to attain better switching characteristics. Further, by the virtue of the piezoelectric response, piezoelectric charges appear at both the top and the bottom surfaces of the channel and only a dual-gate structure can effectively control the electric field at each surface which determines the channel current and its modulation from the induced piezoelectric charges. Therefore, a complete analytical model with dual-gate structure and its validation with experimental results are essential. While analytical models for dual gate TFTs are available,[10] device models that incorporate the effect of piezoelectricity have not been developed or reported. A predictive analytical model can help clarify the mechanism for device operation and aid in expanding their development and applications.[3]

In this work, we report the fabrication and characterization of dual-gated piezoelectric TFTs along with an analytical model

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DOI: 10.1002/admt.202100224

that accurately predicts the current modulation and force responses for independently biased gate electrodes. To understand the force response of the TFT, a simplified 1D charge distribution model was used to calculate the shift in the band-edge profiles induced by the piezoelectric charges, and accounts for surface accumulation and bulk channels. Finally, the response amplitude and polarity were shown to strongly correlate with the biasing regime defined by the gate voltages on both sides of the channel and with the quality of the material at either interface.

2. Results and Discussion

2.1. Fabrication of Dual Gate ZnO Thin Film Transistor

Figure 1a shows the vertical cross section of the dual-gated piezoelectric ZnO TFT. The fabrication was performed on spin-cast polyimide layer on a Si carrier wafer. A single Cr metal was used for the bottom gate and Cr/Au was used for the top gate with Cr facing the channel and atomic-layer deposited Al_2O_3 layers served as the bottom and top gate dielectric layers. The ZnO channel was deposited by low-pressure radio-frequency (RF) magnetron sputtering at the temperature of 200 °C. The deposition time usually ranged from 30 to 40 min to calibrate the thickness of the film that can simultaneously achieve a strong piezoelectric response and efficient gate control of the channel electrostatics.[6] To create Ohmic contacts with a low contact resistance, indium tin oxide (ITO) with a thickness of 80 nm was used as an interface contact material to the ZnO. The entire structure was passivated by a parylene C and a polydimethylsiloxane (PDMS) layers, and Cr/Au leads and pads were connected to the source, drain, and both gates for ease of electrical access. Once the fabrication was completed, the device structure was released from the Si carrier wafer by mechanical peel-off. Figure 1b shows the optical microscope image of the fabricated device, showing the device and the four leads used to access the source, drain, top, and bottom gate electrodes. The channel width/length were 500 µm/50 µm.

We measured the typical output and transfer characteristics of the TFT using the test device on the same wafer in the dual-gate configuration where top and bottom gate electrodes were lithographically connected. Figure 1c shows the output curves of the device, measured by sweeping the drain bias from 0 to 10 V for the gate biases in the range of 0 to 10 V at steps of 2 V with respect to the source. We observed a linear current increase at small drain biases, and channel pinch-off at high drain biases indicative of the formation of a low-resistance ohmic contact and typical n-type semiconducting behavior of the channel. Figure 1d shows the transfer curves measured by sweeping the gate bias from −10 to 10 V at fixed drain biases of 1, 2, and 3 V. The dual gate structure exhibited adequate electrostatic control over the channel with I_{max}/I_{min} ratio exceeding 10^7. The peak field-effect mobility extracted from the transconductance in the linear regime (V_d = 1 V) was 5.08 $cm^2\ V^{-1}s^{-1}$ and the average mobility was 2.39 $cm^2\ V^{-1}s^{-1}$ for V_g in the range of 0–10 V. The subthreshold slope (SS) was extracted to be ≈700 mV dec^{-1}. The gate leakage current was in the order of a 0.1 nA or smaller as illustrated in Figure 1d.

To assess the uniformity of the device properties, we further measured the transfer characteristics of multiple test devices

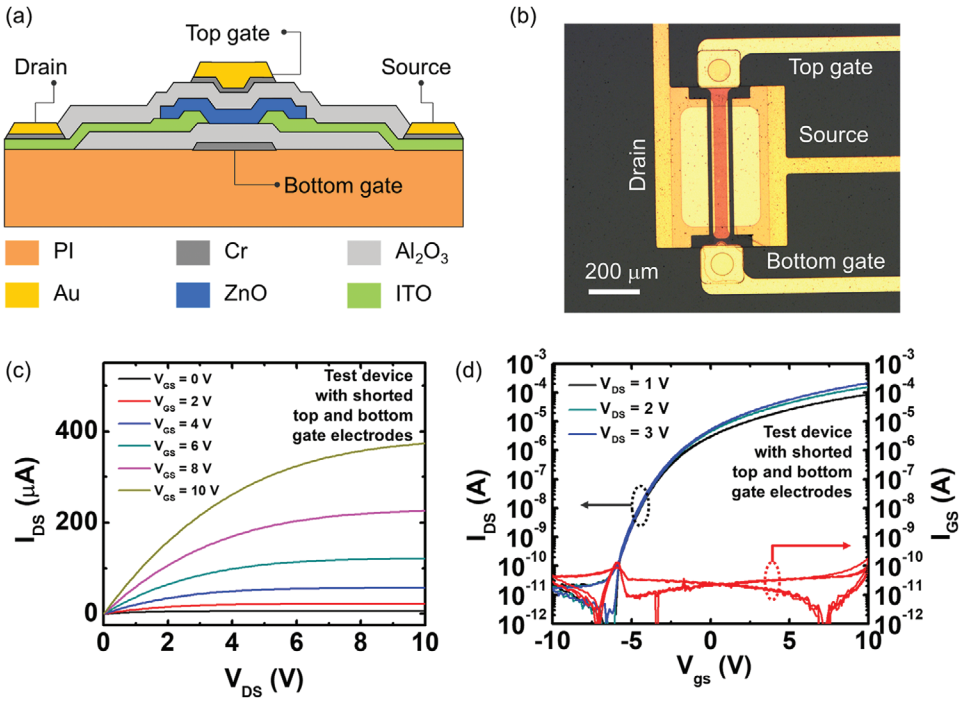

Figure 1. Dual-gate ZnO TFT. a) Schematic illustration of the structure of the dual-gate ZnO TFT. b) Optical microscope image of the fabricated device. Electrical characteristics of the TFT, c) output, and d) transfer curves.

from the same or different wafers. Figure S1, Supporting Information shows the variation of transfer characteristics as a function of location on the wafer, channel length, or oxygen flowrate during the ZnO sputtering. Overall, the transfer characteristics were uniform across multiple parameters, indicating that the fabrication of ZnO dual gate TFTs is reliable and robust.

2.2. An Analytic Model for a Dual Gate TFT in the Linear Regime

To model the current modulation in a dual-gate ZnO TFTs, three semiconductive channels—bulk channel, top accumulation channel, and bottom accumulation channel—should be considered, as schematically illustrated in **Figure 2**a. The following parameters and assumptions were used in this model. The ZnO film is considered to have a thickness of a, width of w, and length of l. The doping level and electrical permittivity of the film are denoted as N_D and ε_s, and assumed to be uniform across the film. The film capacitance, when it is fully depleted, is given as $C_s = \varepsilon_s / a$. The mobility in the bulk of the channel, at the top and the bottom channels are denoted as μ_0, μ_1, and μ_2, respectively. The thickness and permittivity of the dielectrics were denoted as d_i, ε_i and the gate capacitance value is subsequently equal to $C_i = \varepsilon_i / d_i$. (i corresponds to the location of the gate, 1 for top gate and 2 for bottom gate). The voltage biases applied to the top and bottom gates are denoted as V_1 and V_2, respectively. For simplicity, we assume that the drain bias V_D is small and the channel is a linear resistor where the resistance is modulated by the configuration of dual gate biases.

We classify five different possible operation regimes depending on the voltage combinations at the two independent gate electrodes. These regimes can be distinguished by the existence of a bulk channel and a top, a bottom, or both accumulation channels, or the full depletion of the film. Figure 2b illustrates these configurations as a function of top and bottom gate biases, derived by solving the 1D Poisson equation. The following section describes each configuration and its corresponding bias conditions. For simplicity, we have assumed that $V_1 \geq V_2$. The current expressions for the opposite case ($V_2 > V_1$) can be easily obtained by switching V_1 and V_2 and the corresponding parameters.

2.2.1. Two Accumulation Channels and a Fully Conductive Bulk Channel

If the two gate biases are greater than the corresponding flat band voltages, each gate induces the formation of an accumulation channel as shown in Figure 2c(I). The electric fields from the top and bottom gate electrodes are shielded by electron

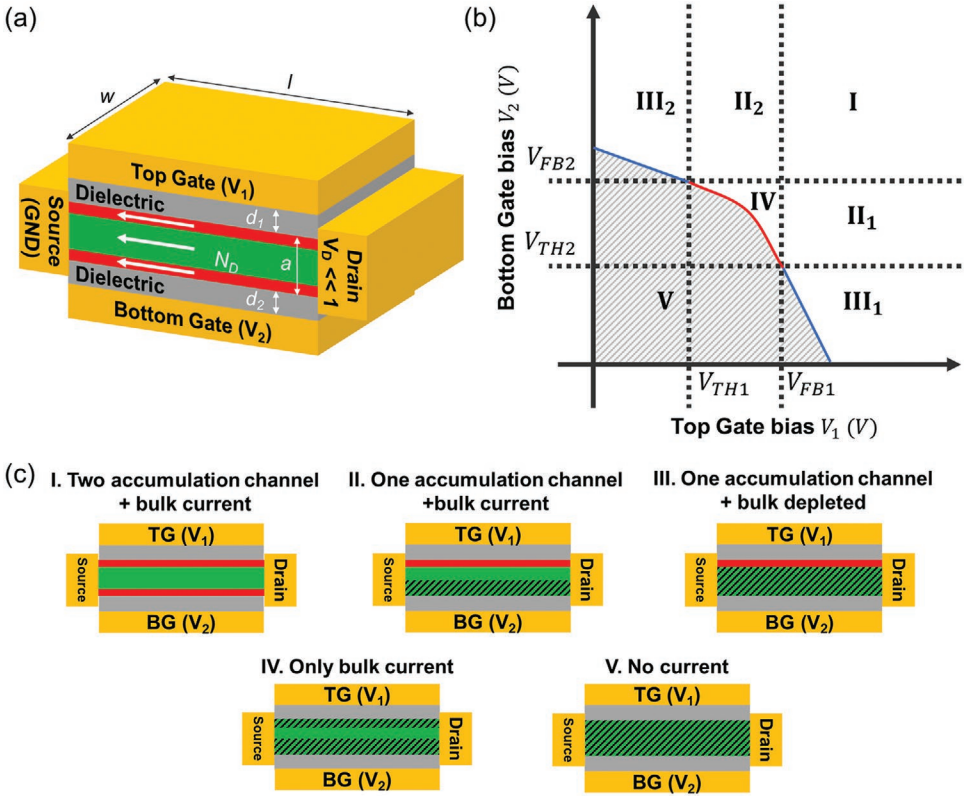

Figure 2. Construction of the analytical model of the dual-gated TFT. a) Schematic illustration of the model, showing top and bottom surface channel, bulk channel, and important parameters. b) Diagram showing different conduction regions. c) Representative channel configurations under different gate bias conditions. I) Both the surface channels and the bulk channel are formed. II) One accumulation channel and bulk channel with partial depletion is formed. III) One accumulation channel while the bulk is fully depleted. IV) Only bulk current exists with partial depletion, while both surface channels are depleted. V) Channel is fully depleted and no current flows.

Table 1. Conditions for the formation of bulk and accumulation channels.

Voltage criteria	Expressions for the current at each channel	
$V_1 > V_{FB1}$ $V_2 > V_{FB2}$	$I_{TC} = V_D\left[\left\{\frac{w}{l}\mu_1 C_1(V_1 - V_{FB1})\right\}^{-1} + 2\{r_f + r_c \exp(-kC_1(V_1 - V_{FB1}))\}\right]^{-1}$ $I_b = V_D\left[\left(\frac{w}{l}\mu_0 V_D aqN_D\right)^{-1} + 2\{r_f + r_c \exp(-kaqN_D)\}\right]^{-1}$ $I_{BC} = V_D\left[\left\{\frac{w}{l}V_D\mu_2 C_2(V_2 - V_{FB2})\right\}^{-1} + 2\{r_f + r_c \exp(-kC_2(V_2 - V_{FB2}))\}\right]^{-1}$	(1)
$V_1 > V_{FB1}$ $V_{TH2} < V_2 < V_{FB2}$	$I_{TC} = V_D\left[\left\{\frac{w}{l}\mu_1 C_1(V_1 - V_{FB1})\right\}^{-1} + 2\{r_f + r_c \exp(-kC_1(V_1 - V_{FB1}))\}\right]^{-1}$ $I_b = V_D\left[\left\{\frac{w}{l}\mu_0(a - W_1)qN_D\right\}^{-1} + 2\{r_f + r_c \exp(-k(a - W_1)qN_D)\}\right]^{-1}$ $I_{BC} = 0$	(2)
$V_1 > V_{FB1}$ $V_2 < V_{TH2}$	$I_{TC} = V_D\left[\begin{array}{c}[\frac{w}{l}\mu_1\{C_1(V_1 - V_{FB1}) - \frac{C_2C_s}{C_2 + C_s}(V_{TH2} - V_2)\}]^{-1} + \\ 2\{r_f + r_c \exp(-kC_1(V_1 - V_{FB1}) + \frac{kC_2C_s}{C_2 + C_s}(V_{TH2} - V_2))\}\end{array}\right]^{-1}$ $I_b = 0$ $I_{BC} = 0$ $I_{TC} = 0$	(3)
$V_1 < V_{FB1}$ $V_2 < V_{FB2}$ $W_1 + W_2 < a$	$I_b = V_D\left[\begin{array}{c}\left\{\frac{w}{l}\mu_0(a - W_1 - W_2)qN_D\right\}^{-1} \\ +2\{r_f + r_c \exp(-k(a - W_1 - W_2)qN_D)\}\end{array}\right]^{-1}$ $I_{BC} = 0$	(4)
$V_1 < V_{FB1}$, $V_2 < V_{FB2}$ $W_1 + W_2 > a$ or $V_1 \geq V_{FB1}$, $V_2 < V_{FB2}$ $C_1(V_1 - V_{FBI}) \leq \frac{C_2C_s}{C_2 + C_s}(V_{TH2} - V_2)$	$I_{TC} = 0$ $I_b = 0$ $I_{BC} = 0$	(5)
Expressions for depletion width and threshold voltage		
	$W_i = -\frac{\varepsilon_s}{C_i} + \left[\left(\frac{\varepsilon_s}{C_i}\right)^2 + \frac{2\varepsilon_s}{qN_D}(V_{FB} - V_i)\right]^{\frac{1}{2}}$ ($i = 1$ or 2)	(6)
	$V_{THi} = V_{FBi} - \frac{qN_D}{2\varepsilon_s}\left(a^2 + 2a\frac{\varepsilon_s}{C_i}\right)$ ($i = 1$ or 2)	(7)

accumulation channels, and no depletion region is induced in the bulk channel. The accumulation current is determined by the excess voltage with respect to the flat band voltage at the corresponding metal–insulator–semiconductor (MIS) interface. The total current in the device is the sum of the bulk current and currents in top and bottom accumulation channels as shown in Equation (1) in **Table 1**.

2.2.2. One Accumulation Channel and Partially Depleted Bulk Channel

If one gate is held positive and the other gate is held negative with respect to the corresponding flat band voltages, there is an introduction of a depletion region in the film due to the negative gate bias as shown in Figure 2c(II). Here, the thickness of the

depletion region, the depletion width W_i, is expressed in Equation (6) of Table 1. If the negative bias is not high enough, the depletion thickness does not exceed the total thickness of the film and bulk current still exists. The accumulation channel at the other side will not be affected by the negative gate bias since the electric field due to the negative bias terminates at the edge of the depletion width where it flips to be become negative with the presence of accumulation charges. The total current is expressed in Equation (2) of Table 1, which is the sum of the current in the accumulation channel, and the current in the bulk channel where the effective thickness is the total thickness minus the depletion width.

2.2.3. Only One Accumulation Channel

Continued from the case II, at a higher negative gate bias, the entire film is depleted except for the accumulation channel on the opposing end to the gate. The positive electric field in the channel begins to reduce the charges in the accumulation channel at the opposing side as shown in Figure 2c(III). This happens when the negative gate bias is smaller than V_{TH2}, expressed in the Equation (7) of Table 1, which corresponds to the voltage at which $W_2(V_2) = a$. The thickness of the accumulation layer is assumed infinitely small. Since the entire film is depleted, the capacitance of the negatively biased gate electrode seen from the accumulation channel is equal to the series combination of C_2 and C_s, $\frac{C_2C_s}{C_2+C_s}$. The total charge in the accumulation channel, expressed in Equation (3) in Table 1, is the sum of the negative charge induced by the positively biased gate, subtracted from the positive depletion charge density induced by the negatively biased gate. It is worth noting that in this charge-sheet model that the thickness of the accumulation channel is infinitely small, that is, assumed to have a zero thickness.

2.2.4. Bulk Only Channel

When both gates are negatively biased, the depletion region is introduced from each side as shown in Figure 2c(IV), giving rise to W_1 and W_2. If the film is not fully depleted ($W_1 + W_2 < a$), there exists a bulk current in the film with an effective thickness of $a - (W_1 + W_2)$. Equation (4) in Table 1 describes the current for this condition.

2.2.5. No Channel

There are two conditions under which the channel can be fully depleted where current flow is prohibited as shown in Figure 2c(V). The first condition is when both gate biases are sufficiently negative such that the sum of the depletion widths exceed the thickness of the film, that is, $W_1 + W_2 \geq a$. The boundary of $W_1 + W_2 = a$ is marked as a red line in Figure 2b. The second condition is when one gate bias is positive and the other gate bias is negative with respect to the corresponding flat band voltages, but the negative bias is high enough to deplete the entire accumulation channel. This condition is described by $C_1(V_1 - V_{FB1}) \leq \frac{C_2C_s}{C_2+C_s}(V_{TH2} - V_2)$. The boundary conditions of $C_i(V_i - V_{FBi}) \leq \frac{C_jC_s}{C_j+C_s}(V_{THj} - V_j)$ ($i = 1$ and $j = 2$ or $i = 2$ and $j = 1$) are marked as blue lines in Figure 2b.

2.2.6. Accounting for the Contact Resistance

The contact resistance must be accounted for in the model because it can be greater than the channel resistance in some operation regimes and it can be modulated by the gate bias in oxide and 2D material based TFTs, the extraction of contact resistance for different gate bias generally exhibits an exponential decrease with the gate overdrive voltage.[7,11,12] At the metal–semiconductor contact interface, a Schottky barrier is formed with a relatively fixed barrier height but a barrier width and trap-levels in the oxide that can be both modulated with the gate voltage. With the relatively high-doping density in the TFT channel, the electron transport across this interface can be described by Fowler–Nordeim tunneling current.[13] As such, the contact resistance is generally observed as an exponential function of the gate overdrive voltage. Our model accounts for this behavior and further isolates the contact resistances, R_{TC}, R_b, and R_{BC} for the top accumulation channel, the bulk channel, and the bottom accumulation channel, respectively. This assumption is schematically illustrated in Figure S2a, Supporting Information. Given that surface accumulation of electrons occurs at either surface of the TFT channel, the R_{TC} and R_{BC} are expected to be much lower than the R_b. Therefore, we can safely ignore the impact of R_b as most of the current will flow near the surface in the on-state of the device. The equation for the contact resistance has the same functional dependence for all three contact resistances and can be expressed as $r_f + r_c e^{-kQ}$. Here, r_f is the voltage independent fixed resistance, which is attributed to the finite conductivity of the contact material. r_c is the maximum contact resistance which is attributed to the Schottky barrier. k determines how fast the resistance decays. Q is the amount of charge per unit area in the corresponding channel (top, bulk, bottom). Q is simply related to the gate overdrive voltage by the gate capacitance, whether top or bottom. The following table summarizes the equations for the current at each channel, I_{TC}, I_b, and I_{BC}, for top accumulation, bulk, and bottom accumulation channel, respectively, under small V_D and voltage criteria for gate biases. The total drain current I_D is given as $I_D = I_{TC} + I_b + I_{BC}$.

2.3. Extraction of Device Parameters and Fitting the Model to Experimental Results

The analytical model makes use of device parameters directly extracted from the experimental results. The cross-sectional FE-SEM image in **Figure 3**a shows the thickness of the ZnO film, sandwiched by the Al_2O_3 dielectric layers, and the gate electrodes. Notably, the ZnO film exhibited a rough top surface resulting in a non-uniform thickness ranging from 59 to 110 nm due to variation in size and height of the coalesced ZnO grains. We used an average of 80 nm as a representative thickness of the film. The top and bottom dielectric layers showed uniform thicknesses, which was confirmed to be 52 and 46 nm, respectively. Other device dimensions such as the channel length or width were taken from design parameters. It should be noted that a relatively high surface roughness is a result from the formation of nanosized grains. The film thickness was slightly higher than usual for this particular

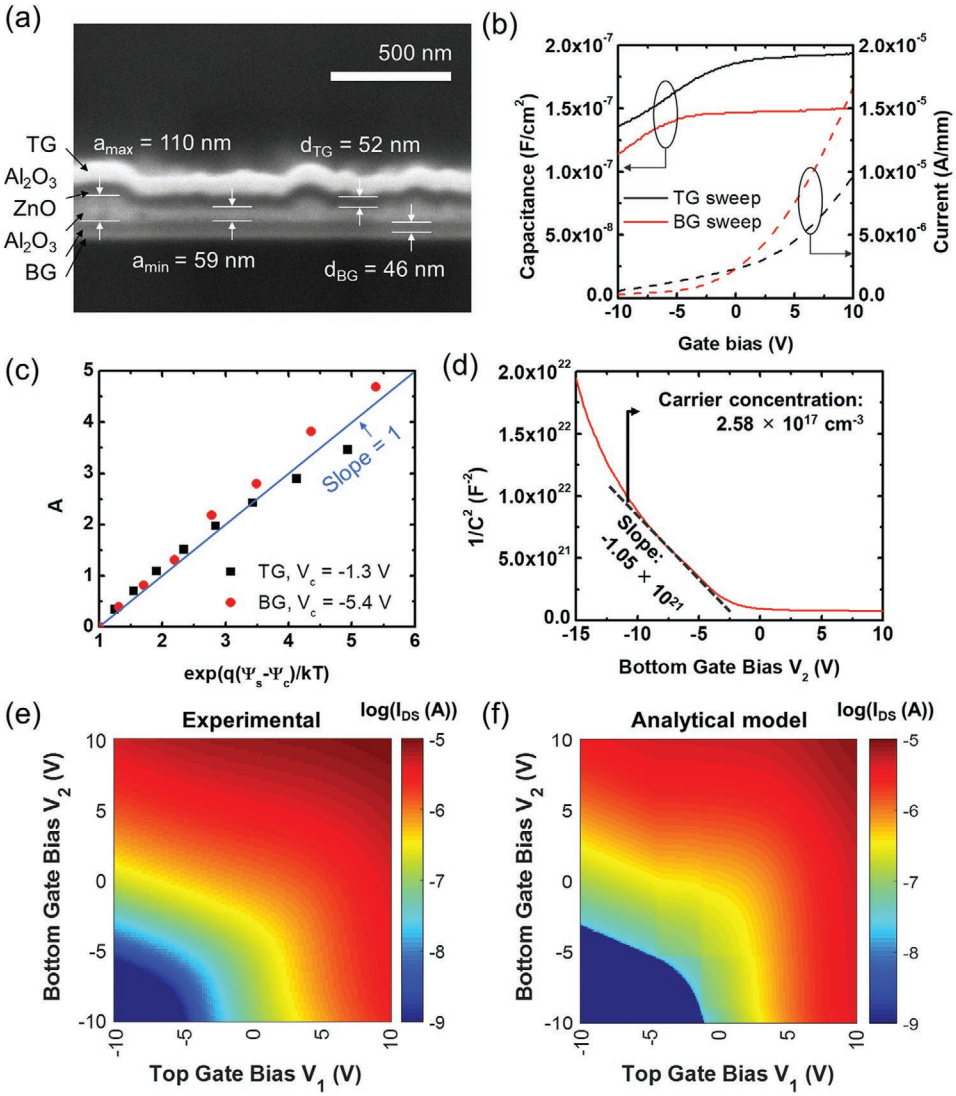

Figure 3. Parameter extraction and model fitting. a) Cross-sectional FE-SEM image of the dual-gate TFT. b) *C–V* curves (solid) and *I–V* curves (dashed) sweeping top (black) and bottom (red) gate while keeping the other gate at zero bias. For *C–V*, the excitation frequency was 10 kHz. For *I–V*, the drain bias was 0.1 V. c) *A* versus $e^{q(\psi_s-\psi_c)/kT}$ plot, obtained from *C–V* and *I–V* curves of sweeping top (black) and bottom (red) gate. V_c of −1.3 and −5.4 V were used to calculate the quantities with respect to the top and bottom gate interfaces, respectively. d) $1/C^2$ plot from the *C–V* curves of the bottom gate while the top gate was grounded. 100 kHz of signal frequency was used. e) The current heatmap generated by the analytical model with the same biasing conditions as the experimental results. f) Current heatmap with top and bottom gate voltages swept independently from −10 to 10 V. A V_{DS} of 0.1 V was used. The device measured in Figure 3e is different from that of Figure 1c,d.

device which resulted in a threshold voltage that is lower than the test devices discussed above.

To extract the flat band voltages, both *C–V* and *I–V* characteristics were utilized to correlate the surface potential and the channel conductance, following methods described in the reference.[14] Figure 3b shows the *C–V* curves (solid lines) and *I–V* transfer curves (dashed lines) corresponding to the sweeping of top (black) or bottom (red) gate biases, respectively. The other gate was grounded during the measurement. Figure 3c shows the *A* versus $e^{q(\psi_s-\psi_c)/kT}$ plot for top gate sweep (black) and bottom gate sweep (red), where *A* is $\frac{C_{ox}a}{\varepsilon_s G_c}\frac{dG}{d\psi_s}[V_{GS}-V_c-(\psi_s-\psi_c)]$. Here, V_{GS} is the gate bias, V_c is an arbitrarily selected bias, ψ_s and ψ_c are corresponding surface potentials, respectively, *G* is the channel conductance for a given gate bias, and G_c is the channel conductance at a gate bias of V_c. For proper choice of $V_c = V_{FB}$, the slope of *A* versus $e^{q(\psi_s-\psi_1)/kT}$ becomes 1. The scatter plots were generated from the choice of V_c of −1.3 and −5.4 V for top and bottom gate sweeps, respectively, indicating that these values can be used as flat band voltages of corresponding gate electrodes.

For the gate oxide capacitances, we used the maximum measured values of the *C–V* curves. This led to the higher top gate oxide capacitance of 1.94×10^{-7} F·cm^{-2} while that of the bottom gate was measured to be 1.50×10^{-7} F·cm^{-2}. The rough morphology of the top surface of the ZnO film resulted in a larger surface area leading to a higher capacitance. The measured capacitance and thickness values yielded the relative Al_2O_3

Table 2. Parameters used in the analytic model.

Variable	Parameter	Value	References
V_{FBj}	Flat-band voltage	$V_{FB_1} = -1.3$ V $V_{FB_2} = -5.4$ V	From *C–V* curves
a	Thickness of the channel	80 nm	Measured from the SEM image
C_j	Capacitance of gate electrode per unit area	$C_1 = 1.94\times 10^{-7}$ F·cm^{-2} $C_2 = 1.50\times 10^{-7}$ F·cm^{-2}	From *C–V* curves
d_j	Thickness of the gate insulator	$d_1 = 52$ nm $d_2 = 46$ nm	From the calibration sample
ε_j	Permittivity of the gate insulator	$\varepsilon_1 = 11.5\varepsilon_0$ $\varepsilon_2 = 7.8\varepsilon_0$	Calculated from C_j and d_j
l	Length of the channel	50 mm	Design parameters
w	Width of the channel	500 mm	Design parameters
ε_s	Permittivity of the semiconductor	$8.5\varepsilon_0$	From the literature[16]
μ_0	Electron mobility	2.39 cm^{2}V^{-1}s^{-1}	Calculated from the test device (Average value for $V_g = 0$–10 V)
N_D	Doping concentration of the semiconductor	2.5×10^{17} cm^{-3}	From *C–V* curves (Mott plot)
r_f	Field-independent contact resistance	1000 Ω	From our prior work[7]
r_c	Maximum contact resistance from the Schottky barrier	1.5×10^6 Ω	From our prior work[7]
k	Characteristic speed for contact resistance decay	3.5×10^6	From our prior work[7]

permittivity to be 11.5 and 7.8 for top and bottom dielectrics, respectively.

The doping concentration of the film was extracted by plotting the $1/C^2$ measured from the bottom gate with flat surface, as shown in Figure 3d. The $1/C^2$ plot showed an expected linear dependence in the depletion regime in the V_g range of –4 to –8 V, and the slope resulted in the doping concentration of 2.5×10^{17} cm^{-3}. Other parameters such as permittivity of ZnO channel were taken from the literature.[15] For the mobility, we used the average field effect mobility of 2.39 cm^2 V^{-1}s^{-1} in the V_g range of 0 to 10.

Finally, parameters for modeling the contact resistance were chosen to mimic the actual change of the measured contact resistances. Figure S2b, Supporting Information shows the plot of the contact resistance as a function of gate bias (shorted top and bottom gate electrodes), from experimental results of previously reported work[7] and for the charge-exponential analytical model for top and bottom accumulation channels as described above. The experimental result from a TFT which showed similar threshold voltage (5% of O_2 partial pressure) to this study was used for this extraction. The exponential decrease of the contact resistance is well reproduced by the model. All parameters used in the computation of the device current according to the model are summarized in **Table 2**.

To validate this model for all operating regimes, we first measured the drain current at V_D = 0.1 V while sweeping the top and bottom gate electrodes from –10 to 10 V, independently. The colormap in Figure 3e shows the log(I_D) values as a function of the top and bottom gate biases (V_1 and V_2, respectively), for a device that had its top and bottom gate electrode independently controlled, different from that of Figure 1 which had both gates simultaneously connected to the same pad. There was a negligible current (<1 nA) at the lower left corner of the graph where both V_1 and V_2 were negatively biased smaller than –5 V, indicating that the channel was completely turned off. The current increased exponentially with respect to the increase of either V_1, V_2, or both. The contour lines are straight for different V_1 and V_2 but became rounded when they approached a similar level, as predicted. There is however asymmetry in the gate effects that is due to the fact that the film quality at the bottom interface at the onset of the ZnO deposition is usually poorer than the top-surface film quality.[6]

The analytical solution with the experimental parameters and assumptions plotted in Figure 3f successfully replicated those experimentally measured and plotted in Figure 3e. The current changes with respect to V_1 and V_2 were similar to the experimental data in Figure 3e, including identical turn off when both gates are negatively biased, gradual exponential increase when both gates are positively biased, and a curved contour near V_1 = 0–5 V and V_2 = –10 V (and vice versa). The sudden decrease of the current in the negative bias region (lower left) is due to the absence of a subthreshold current component in the analytical model described here. The sensor elements that are addressed within a matrix array of piezoelectric TFTs need to operate in the on-state, and therefore, we precluded the subthreshold operation from our analysis. Additionally, the calculated contours from the analytical model are more symmetric than the experimental ones because the material thicknesses and qualities are not perfectly symmetric in the experiment. Overall, the model successfully predicted the behavior of the dual gate TFT.

2.4. Effect of Piezoelectric Charges in Dual-Gate TFT

The force response of the ZnO TFT comes from the interaction between the force-induced piezoelectric charges and the gate-induced accumulation of electron charge density, as illustrated schematically in **Figure 4**a. The piezoelectric field alters the

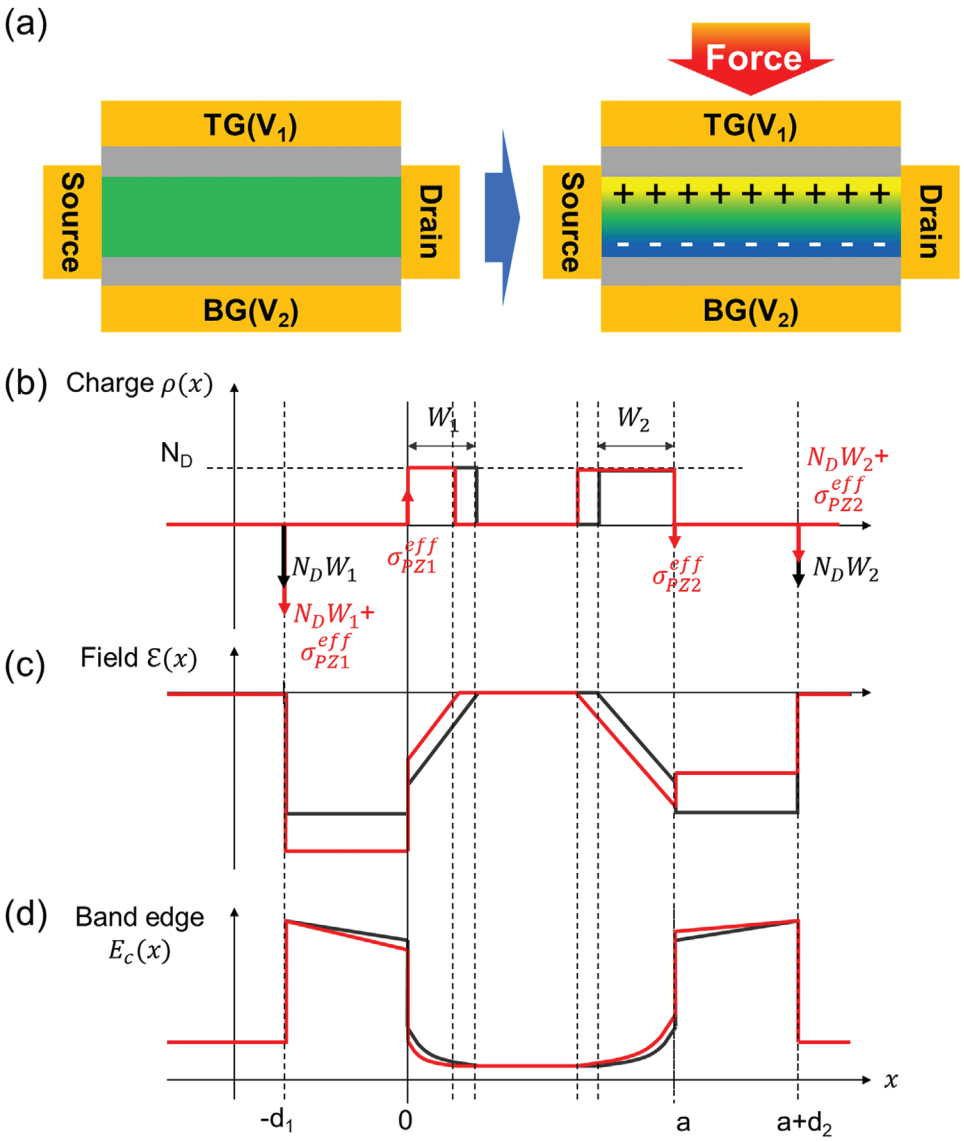

Figure 4. Force response of the dual gate TFT explained by a 1D charge distribution model. a) Illustration of the force response mechanism of the TFT. Plots of b) charge density, c) electric field, and d) band-edge profile across the channel based on the simplified 1D model. Black lines and red lines correspond to plots before and after force application, respectively.

distribution of the electric potential inside the film, shifting the flat band voltage (V_{FBi}). This shift alters the free carrier density in the channel which in turn changes the total current of the TFT. To calculate the piezoelectric-induced shift in the flat-band voltage at each surface of the thin film, we use a simplified 1D model for charge distribution as shown in Figure 4b. In this model, piezoelectric charges are considered as a thin sheet of charges with a zero thickness, which appears at both the top and bottom surfaces with opposite polarity. Ideally, the amount of the piezoelectric charges at each surface should be equal. However, RF-magnetron sputtered ZnO thin films have higher density of defects at the bottom surface originating from the non-epitaxial surface of the disordered Al_2O_3 dielectric layer underneath and from multiple granular nucleates, and a lower defect density at the top surface where the grains coalesce with each other. Therefore, we have included the factors r_1 and r_2 which assume values between 0 and 1, representing the amount of effective piezoelectric charges at either surface, that is, $\sigma_{PZ1}^{eff} = r_1\,\sigma_{PZ1}$ and $\sigma_{PZ2}^{eff} = r_2\,\sigma_{PZ2}$.

The piezoelectric field will re-distribute the neighboring charge density in the channel since the voltage at both gate electrodes is kept constant. Solving the Poisson's equation gives the expressions for charge density $\rho(x)$, electric field $\varepsilon(x)$, and electric potential $\Phi(x)$ as a function of position x, as summarized in the **Table 3**.[9] $\rho(x)$, $\varepsilon(x)$, and the energy band edge profiles calculated from $\Phi(x)$ are plotted in Figure 4b–d.

With the existence of piezoelectric charges, the voltage drop across the gate dielectric layer and the depletion region is given by:

$$V_i = \frac{q}{\varepsilon_s}\left(N_D W_i + \sigma^{PZ}\right) d_i + \frac{q}{2\varepsilon_s}\left(N_D W_i^2\right) \tag{8}$$

Table 3. Conditions for the formation of bulk and accumulation channels.

x	$\rho(x)$	$\varepsilon(x)$	$\Phi(x)$
$x < -d$	0	0	V_1
$-d \le x < 0$	$(N_D W_1 + \sigma_{PZ1}^{eff})\delta(-d)$	$-\frac{q}{\varepsilon_1}(N_D W_1 + \sigma_{PZ1}^{eff})$	$\frac{q}{\varepsilon_1}(N_D W_1 + \sigma_{PZ1}^{eff})(x + d_1) + V_1$
$0 \le x < W_1$	$\sigma_{PZ1}^{eff}\delta(0) + N_D$	$-\frac{q}{\varepsilon_s}(N_D W_1 - N_D)x$	$\frac{q}{\varepsilon_1}(N_D W_1 + \sigma_{PZ1}^{eff})d_1 + \frac{q}{\varepsilon_s}N_D\left(W_1 x - \frac{x^2}{2}\right) + V_1$
$W_1 \le x < a - W_2$	0	0	$\frac{q}{\varepsilon_s}(N_D W_1 + \sigma_{PZ1}^{eff})d_1 + \frac{q}{2\varepsilon_s}N_D W_1^2 + V_1 = 0$
$a - W_2 \le x < a$	N_D	$-\frac{q}{\varepsilon_s}N_D(x - a + W_2)$	$\frac{q}{\varepsilon_2}(N_D W_2 + \sigma_{PZ2}^{eff})d_2 + \frac{q}{\varepsilon_s}N_D\left(W_2(a-x) - \frac{(a-x)^2}{2}\right) + V_2$
$a \le x < a + d$	$\sigma_{PZ2}^{eff}\delta(a)$	$-\frac{q}{\varepsilon_2}(N_D W_2 + \sigma_{PZ2}^{eff})$	$-\frac{q}{\varepsilon_2}(N_D W_2 + \sigma_{PZ2}^{eff})(a - x + d) + V_2$
$a + d \le x$	$(N_D W_2 + \sigma_{PZ2}^{eff})\delta(a + d)$	0	V_2

for ($i = 1$ or 2). Solving Equation (7) for W_i, we obtain:

$$W_i = -\frac{\varepsilon_s}{C_i} + \sqrt{\frac{2\varepsilon_s}{qN_D}\left(V_{FB} - V_i - \frac{\sigma_{PZi}^{eff}}{C_1}\right) + \left(\frac{\varepsilon_s}{C_i}\right)^2} \tag{9}$$

Equation (8) indicates that effectively, the flat-band voltage shift, V_{FBi}^{PZ}, due to the piezoelectric charge density can be expressed as follows:

$$V_{FBi}^{PZ} = V_{FBi} - \frac{\sigma_{PZi}^{eff}}{C_i} \tag{10}$$

We can now substitute V_{FBi} with V_{FBi}^{PZ} in the analytical solution in Table 1 to obtain the current in the dual gate TFT under the presence of piezoelectric charges in response to force stimuli.

2.5. Field Tunable Piezoelectric Response in Dual-Gate ZnO TFT

The electric field-dependent force response of the dual gate ZnO TFT was investigated by measuring the current change under force application for different top and bottom gate biases ranging from –10 to +10 V. Here, a constant force of 50 mN was applied to the TFT using a linear actuator with an integrated force sensor. **Figure 5**a shows the color map for the amplitude of current changes. An increase in the current is observed mainly for a positive top gate bias V_1, regardless of the bottom gate bias V_2. Notably, a higher V_1 resulted in greater current changes, which can be attributed to the larger transconductance of top-gate in the as-fabricated TFT. By contrast, the application of force resulted in a decrease in current when the bottom gate was positively biased, and the top gate was negatively biased. There was almost no response observed when both gates were negatively biased when the TFT was turned off.

We were able to replicate the experimental findings with our model using the following assumptions. First, we assumed positive piezoelectric charges at the top surface and negative charges at the bottom surface. To calculate the piezoelectric charge density, we assumed a 0.09% of the vertical strain in the channel, with a known elastic modulus of 211 GPa, and a piezoelectric coefficient of 12.4 pC N^{-1}.[17,18] We also assumed that only 50% of piezoelectric charge is effective at the bottom surface due to the charge screening by surrounding local defects, that is, r_1 of 1.0 and r_2 of 0.5. The calculated effective piezoelectric charges were then used to calculate the shift in the flat band voltages at each gate using Equation (9). The parameters that were used in this calculation are summarized in **Table 4**.

Figure 5b shows the response colormap from the analytical model. Important features such as a positive response for a positive top gate bias ($V_1 > 0$), negative responses for a high

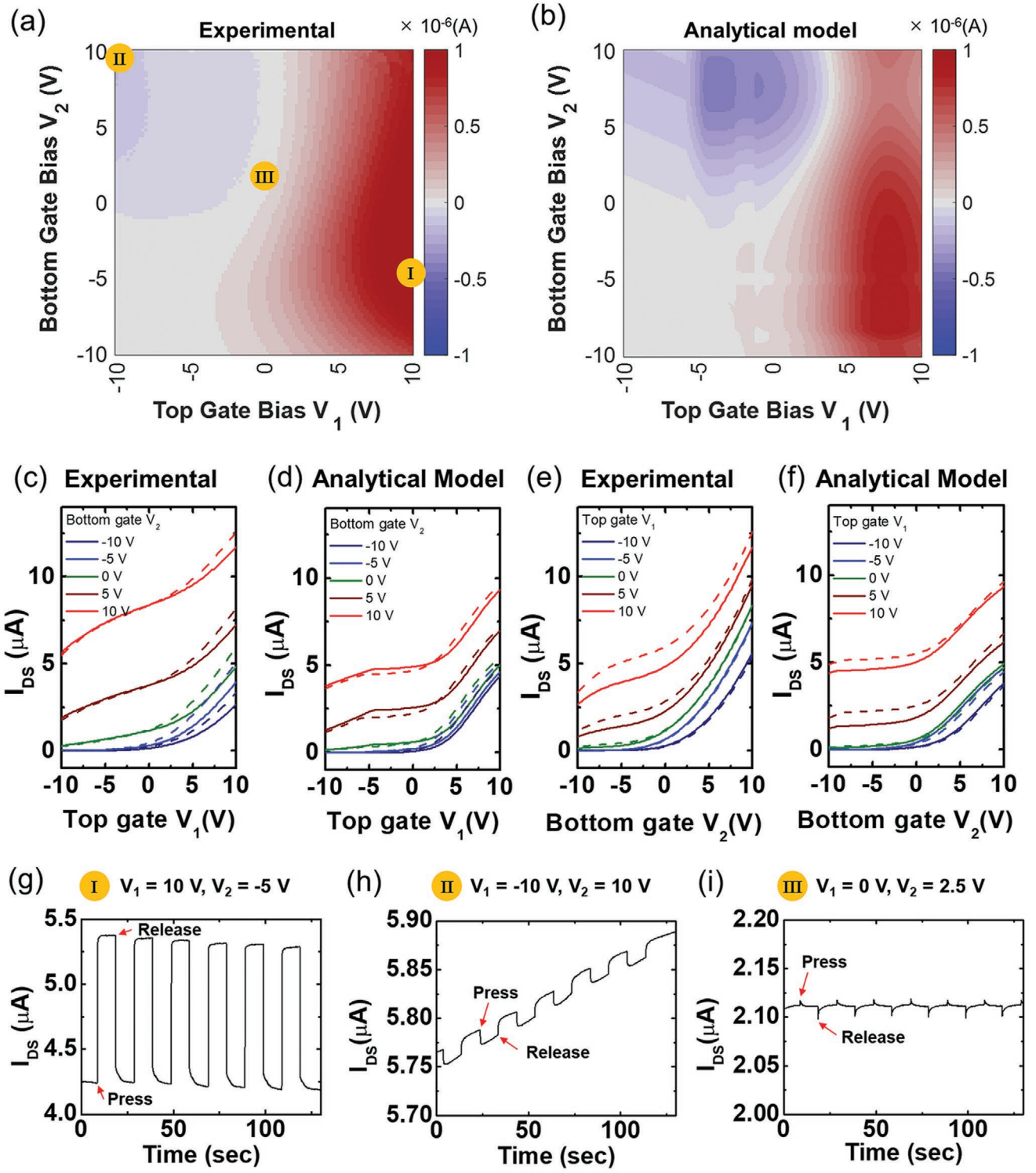

Figure 5. Electric field tunable force response. a) Heatmap plot of the current change induced by the external force. b) The same plot generated by the analytical model. Plots of transfer curves before (dashed) and after (solid) force application, obtained from experiments and calculated from the analytical model. Top gate sweep (V_1) with fixed bottom gate voltage (V_2), c) experimental and d) calculation result. Bottom gate sweep (V_2) with fixed top gate voltage (V_1), e) experimental and f) calculation result. Current versus time curves with force applied and released every 10 sec. Constant force of 50 mN was used. g) When $V_1 = 10$ V and $V_2 = -5$ V, corresponding to the top surface channel dominant configuration. h) $V_1 = -10$ V and $V_2 = 10$ V, corresponding to the bottom surface channel dominant configuration i) $V_1 = 0$ V and $V_2 = 2.5$ V, where the effect from each surface channel is balanced.

Table 4. Parameters used in the analytic modeling of the force response.

Variable	Parameter	Value	Reference
δ_s	Thickness of the piezoelectric charge	0.5 nm	Assumption
ε_3	Strain along the normal direction	0.09%	Assumption
c_{33}	Elastic modulus in c-axis direction	211 GPa	From the literature[17]
d_{33}	Piezoelectric coefficient of ZnO in c-axis direction	12.4 pC N^{-1}	From the literature[18]
σ_{PZi}	Piezoelectric charge density	1.55×10^{12} cm^{-2}	Calculated from ε_3, c_{33} and d_{33}
r_i	Reduction ratio of the back surface piezoelectric charge	$r_1 = 1.0$ $r_2 = 0.5$	Assumption
σ_{PZi}^{eff}	Effective piezoelectric charge density	$\sigma_{PZ1}^{eff} = 1.55 \times 10^{12}$ cm^{-2} $\sigma_{PZ2}^{eff} = 7.75 \times 10^{11}$ cm^{-2}	Calculated from σ_{PZi} and r_i
V_{FBi}^{PZ}	Flat-band voltage under presence of piezoelectric charges	$V_{FB1}^{PZ} = -2.58$ V $V_{FB2}^{PZ} = -1.27$ V	Calculated from the Equation (9)
ΔV_{FBi}^{PZ}	Flat-band voltage shift under presence of piezoelectric charges	$\Delta V_{FB1}^{PZ} = -4.57$ V $\Delta V_{FB2}^{PZ} = 0.83$ V	Calculated from V_{FBi} and V_{FBi}^{PZ}

bottom gate bias ($V_2 > 0$) and negative top gate bias ($V_1 < 0$), and almost no response for zero top gate bias ($V_1 \approx 0$), were well reproduced with a similar response amplitude. We also compared the experimental and calculated transfer curves for both top and bottom gate sweeps with different fixed non-sweeping gate biases. The curves obtained by top gate sweep with fixed bottom gate bias values are shown in Figure 5c (experimental) and Figure 5d (calculation), and curves by bottom gate sweep with fixed top gate biases are shown in Figure 5e (experimental) and Figure 5f (calculation). The transfer curves derived from the analytical model exhibited similar trends as the experimental values, both with and without force application, validating the physics captured by the model.

It is important to note that the 0.09% of the strain corresponds to 200 MPa pressure, which is much greater than the experimentally applied pressure of 16 kPa. We attribute this drastic difference to the fact that the flexible TFT channel initially had a slight bending which is flattened during pressure application; the changes in the curvature of the film can introduce high strain levels. Further analysis including finite element analysis might reveal the mechanical interaction inside and near the device region.

As discussed in the previous section, the response of the TFT can be tuned by the gate biases. We demonstrated this tunable piezoelectric response by measuring the temporal response curves with different bias configurations. The bias regimes marked by I, II, and III in Figure 5a were used for this analysis. In the first configuration (I), $V_1 = 10$ V is applied to the top gate while $V_2 = -5$ V is applied to the bottom gate such that a top-surface channel is formed. The temporal response curve in Figure 5g exhibits a strong positive response under force application. On the other hand, in the second configuration (II), the top gate is negatively biased ($V_1 = -10$ V) while the bottom gate is positively biased ($V_2 = 10$ V), and the effective channel is located near the bottom gate. In this configuration, the response polarity was negative with a reduced amplitude, as shown in Figure 5h. In the third configuration (III), where the top gate is grounded ($V_1 = 0$ V) and bottom gate has a low positive bias ($V_2 = 2.5$ V), the resulting net response was almost zero as shown in Figure 5i. The current increased instantaneously right after the force application, but it recovered to zero with time. These responses in configuration (III) near the weakly-on TFT regime indicate that the transient response is overwhelmed by trap-state charging and discharging, whereas in the strongly-on regime, these effects are mitigated by the large free-carrier density in the channel that surpasses the trap-state effects. Overall, we demonstrated that the piezoelectric response of the TFT can be altered by tuning the gate voltages, as expected, and validated these changes with our physics-based model.

3. Conclusion

In summary, we investigated the current modulation and piezoelectric response of the dual-gate ZnO TFT experimentally and analytically. The dual gate ZnO TFT fabricated on a polyimide substrate exhibited strong current modulation and independent response with top and bottom gate biases. This current modulation behavior was explained well by the analytical model, which accounts for the bulk depletion, conduction, and surface accumulation channels. The analytical model accounts for shifts in the flat-band voltage at each gate interface induced by the piezoelectric field with force application. The experimental piezoelectric response of the dual gate TFT was well reproduced by the analytical model, confirming that our model captures the essential physics of the piezoelectric TFT. Importantly, by adjusting the bias value for each gate, we

were able to control the response polarity and amplitude from –0.29 to 22.7 nA mN^{-1}. This study provides an analytical and intuitive understanding for the operation of a general dual-gated TFT and its piezoelectric device applications, which may contribute to the development of and advancing the applications of novel TFT-based electromechanical sensors. This work will contribute to the development of active force sensors array for a variety of applications, such as robotics, wearable electronics, and Internet of Things.[2]

4. Experimental Section

Fabrication of Dual Gate ZnO Thin Film Transistor: Polyimide layer (PI-2611, HD MicroSystems) was used as a flexible substrate, which was spin-coated on a 4-inch sized bare Si carrier wafer and thermally cured in a convection oven (Carbolite High Temperature Clean Room Oven). To make the bottom gate electrodes, thin Cr layer was deposited on the substrate by DC magnetron sputtering (Denton Discovery 18 Sputter System), followed by photolithography and wet etch processes for patterning. Heidelberg MLA 150 was used for all the photolithography process, and Transene Chromium etchant 1020 was used to etch Cr. For the bottom dielectric layers, Al_2O_3 layer was deposited using atomic layer deposition (ALD) technique (Beneq Atomic Layer Deposition System). The bottom dielectric layers were patterned and wet etched into micro islands to minimize the strain. Buffered oxide etchant 6:1 from Sigma Aldrich which was further diluted with water was used in this process. Afterward, the source and drain electrodes were formed by sputtering of Cr and Au layers followed by photolithography and wet etching. Transene Gold etchants TFA was used for etching Au layer. ITO was deposited as an Ohmic interface layer at room temperature, using RF magnetron sputtering (AJA RF Sputter Deposition System). Photolithography and wet etch using dilute HCl solution was followed to pattern the ITO layer. After patterning, ITO was thermally annealed in N2 environment (Allwin RTA) to improve the conductivity. The ZnO channel layer was deposited using the same RF magnetron sputtering system, at elaborated temperature of 200 °C. After deposition and cooling, the film was immediately passivated with a thin ALD-Al2O3 layer to prevent any degradation from ambient moisture. The film was then patterned using photolithography and wet etch of Al2O3 layers (diluted buffered oxide etchant 6:1) and ZnO layers (diluted HCl solution). For the top dielectric layers, another ALD-Al2O3 layers were deposited. Additional photolithography and wet etch process isolated the dielectric layers to minimize the strain and avoid cracks. For the top gate electrodes, Cr/Au leads were deposited with Cr film facing the device using the same DC sputtering system followed by photolithography and wet etch. Finally, the entire structure was passivated by a Parylene C layer, deposited using PDS Parylene Coater. A photolithography and dry etch process (Oxford Plasmalab 80) was followed to expose all the electrodes for further electric connections. Cr/Au leads and pads were connected to the source, drain, and both gates for ease of electrical access, using same DC sputtering and wet etch process. Additional Parylene C layer was deposited for further passivation. Finally, the device was released from the host Si wafer by mechanical peel off and sandwiched between two sheets of PDMS layers which had thickness of 75 mm.

Measurement of DC Characteristics: DC characteristics such as output, transfer, and *C–V* curves of the fabricated TFT were measured using a B1500A semiconductor device analyzer. External force was applied by a voice-coil powered linear actuator system with internally integrated force sensor (V-275 PIMag Voice Coil Linear Actuator). At the tip of the actuator, a custom-made apparatus with a specific surface, machined from acrylic rod, was attached to apply to the TFT of interest. The force response was measured to have an error of around 10%.[7] All measurement was done under the ambient condition.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors acknowledge support from the nano3 fabrication facilities and staff at UC San Diego. The nano3 facility is part of the San Diego Nanotechnology Infrastructure (SDNI) of UCSD, a member of the National Nanotechnology Coordinated Infrastructure, which is supported by the National Science Foundation (Grant ECCS-1542148). This work was supported by NIH Director's New Innovator Award DP2-EB029757 and the National Science Foundation grant CMMI-1728497.

Conflict of Interest

S.A.D. and H.O. are inventors on a U.S. patent application related to this work filed by UC San Diego (no. 63/065,075, filed on 13 August 2020). The authors declare no other competing interests.

Author contributions

S.D. and H.O. conceived the project and designed the experiments; H.O. carried out the experiments and developed the model and analysis with input from S.D.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

force sensors, piezoelectric field-effect transistor, thin film transistors

Received: February 24, 2021
Revised: April 29, 2021
Published online:

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