

Freestanding High-Power GaN Multi-Fin Camel Diode Varactors for Wideband Telecom Tunable Filters

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Abstract—The quality, resolution, and quantity of information transmitted in RF front end modules favor compact tunable filters with varactor elements that can handle high power and that are highly linear. Gallium nitride (GaN) varactors can theoretically reach the highest quality factor figure of merit (QFOM), owing to the GaN outstanding breakdown electric field and good electron mobility. Popularly pursued GaN Schottky diode varactors suffer from leakage currents at high reverse voltage biases at their junctions and because of GaN inherent threading dislocations in thin GaN layers on foreign substrates. We devised a novel device architecture to overcome these limitations. First, we employ an interdigitated anti-series multi-Fin camel diode structure composed of a thin p⁺ GaN top layer situated between the Schottky metal and an n-type GaN drift layer. The anti-series symmetric Fin structure leads to excellent linearity and minimizes device parasitics to achieve measured record high Q factors. The p-GaN layer raises the barrier height to suppress reverse leakage current to maintain a high Q factor at higher reverse biases than Schottky diodes. Second, we utilize GaN on Qromis Substrate Technology (QST) wafers that permit the growth of thick GaN layers with lower dislocation densities and lower leakage currents than GaN-on-Si and that are comparable to GaN-on-GaN. We report in this work the fabrication and dc, RF S-parameters of these diodes, and assess their potential with empirical models. Breakdown voltage of 146 V and extrapolated Q factor of 84, 33, and 9 at 2, 5, and 18 GHz, respectively, are obtained in multi-Fin back-to-back varactor device configuration.

Index Terms—Camel diode, GaN varactor, high breakdown voltage, quality factor, RF adaptive circuit.

I. INTRODUCTION

CTIVE and passive circuit miniaturization has fueled the ever-increasing speed and bandwidth of RF front-end modules both in mobile devices and base stations. Mobile systems as 4G LTE, 5G NR, and more advanced radio access technologies utilize multiple distinct bands that must

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be supported with minimal interference, along with Bluetooth, Wi-Fi connectivity, and GPS. With a wider frequency bandwidth, the complexity of RF front-end architecture and the density of passive elements of an RF board will increase [1], [2]. Additionally, to offer high-speed data regardless of user location with less RF signal loss at high frequency, base stations are expected to be seamlessly placed in dense cells, in close proximity to users. Accordingly, the size and weight of future base stations should be decreased [3], [4]. Multiband tunable filters are useful to select distinct signal frequency ranges for transmission and reception. Although currently band-select filters cannot typically be implemented with tunable technology, the area, weight, and cost challenges for coarse tuning can be addressed by employing adaptive components integrated into compact tunable filters. In addition to applications in tunable filters, adaptive components are essential for tunable matching networks, which are placed between the power amplifier and the antenna. Tunable matching networks that consist of varactor diodes to achieve broadband matching and efficiency improvement have already been reported [5], [6]. While various tunable elements have been proposed, the required criteria of high quality factor (O), high linearity, and high power handling capability for a variety of civilian and military applications are not concurrently satisfied by a single device architecture in available technologies to date.

Tunable element technologies include mechanically tuned dielectric resonator filters [7], [8], tunable superconducting filters [9], p-i-n diode switches [10], [11], barium strontium titanate (BST) capacitors [12], [13], [14], and varactor diodes [15]. The tradeoffs for these tunable elements constrain their applications. For instance, mechanically tuned cavity filters are bulky, and cryogenic coolers are mandatory for the usage of superconducting filters. Compared with p-i-n diode-based tunable filters that have discrete tuning, varactor diodes-based filters offer continuous tuning with better tuning resolution, more compact form factor, and lower power consumption. CMOS varactors have limited power handling prospects and CMOS passive elements also suffer from low quality factor. Although MEMS varactors nowadays suffer less from reliability problems, they can be affected by intermodulation distortion because the modulation envelope of an RF signal can affect the position of the membrane [16]. MEMS varactors are also characterized with a small tuning range and a small capacitance density. BST-based tunable elements achieve high capacitance density, good tuning range

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at low voltages in the range of 1-25 V, and are utilized in IC products. These ICs demonstrate good third-order intercept point (IP3) with input signals of 25 dBm but rather allow a 33-dBm maximum input power [17]. GaN Schottky diode power varactors were envisioned to obviate the limitations of MEMS and BST varactors. GaN is particularly employed because it can reach the highest quality factor figure of merit (QFOM) compared to other semiconductor materials for a given doping profile and device geometry. Earlier work on GaN Schottky diodes with InGaN tunneling barriers achieved a breakdown voltage exceeding 120 V, a Q exceeding 100 at 1 GHz with a tuning range of 3.8:1 [18], [19], [20]. When GaN Schottky diode varactors were employed in an antiseries configuration, the linearity of the varactor was improved, such that an OIP3 of 71 dBm was obtained [21], [22]. However, the devices are fundamentally limited because the GaN material was grown on sapphire substrates, and as a result, the reverse leakage current density exceeded 20 mA/cm² at -50 V. In addition, an increased reverse dc bias did not increase Qas expected and the extracted series resistance rose with bias.

We applied two strategies—simultaneously—to improve leakage current density and breakdown voltage in vertical GaN varactors by leveraging low-defect density GaN by thick epitaxy on engineered substrates, Qromis Substrate Technology (QST), and by implementing the camel diode device architecture [23], [24], [25]. The leakage current density in vertical GaN devices is proportional to the dislocation density, which decreases as the GaN layers become thicker, as well as to the density of defects and impurities in the GaN layers [26]. We have shown in a previous report that Schottky diodes with regrown GaN/QST templates could reach a low dislocation density and a comparable leakage current density to similar sized and manufactured diodes on regrown GaN on freestanding GaN substrates [27]. The camel diode device architecture constitutes a fully depleted p⁺ GaN layer atop n⁻-GaN, which offers an anode barrier height up to 3.4 V, higher than the conventional n⁻-GaN-based Schottky diode, which is characterized with a barrier height of 0.7 V with the welldeveloped Ni contacts. A greater barrier height and a wider tunneling width at the surface of the camel diode can provide low leakage currents. A p-n diode structure with a thicker p⁺ GaN layer can in principle reduce the leakage currents but suffers from losses due to both the poor ohmic contact between the metal and the p⁺ GaN interface [28], [29] and the undepleted p-GaN layer. If a thick p⁺ GaN is utilized in this work, the total series resistance will increase by several times even with a p⁺ GaN contact resistivity of $1 \times 10^{-4} \ \Omega \text{cm}^{-2}$, which is considered as a good resistivity for a p⁺ GaN Ohmic contact [30].

In this work, we first developed and implemented an epitaxial structure for GaN camel diodes on QST substrates and assessed the reliability of device fabrication with circular device architectures. We then developed and optimized antiseries multi-Fin GaN diode varactors and characterized their RF performance with regard to linearity and Q-factor. Similar concepts of multidimensional architectures are widely used in power device applications [31]. The dc characteristics of these circular diodes exhibited excellent uniformity in their current–voltage (I-V) characteristics and consistently a low leakage current density and relatively high breakdown voltage



Fig. 1. Device structure and band diagram schematic of a circular diode. (a) Cross-sectional structure of circular diodes. (b) Schematic of a typical band-edge diagram for Schottky and camel diodes.

in agreement with design concurrently with a robust yield across devices. The dc characteristics of the multi-Fin GaN diode varactors agreed well with those of circular varactors in their capacitance–voltage (*CV*) characteristics in reverse bias but generally exhibited slightly lower breakdown voltages. *S*-parameter measurements were conducted to validate the quality factor features.

II. CIRCULAR DIODES

A. Device Structure and Fabrication Process

The material structure consisted of a top 23-nm p⁺-GaN (Mg doped, $N_A = 2 \times 10^{19}$ cm⁻³) and 1- μ m n⁻-GaN (Si doped, $N_D = 2 \times 10^{17} \text{ cm}^{-3}$) on top of 5- μ m n⁺-GaN (Si doped, $N_D = 2-3 \times 10^{18} \text{ cm}^{-3}$) grown by metal organic chemical vapor deposition (MOCVD) on 6" GaNon-QST substrate template that consisted of 5- μ m n⁻-GaN on nucleation, bonding, and isolation layers on a polycrystalline AlN substrate. The 6" wafer surface was protected with photoresist, which after dicing was dissolved in remover PG (N-methyl-2-pyrrolidone-based solvent) in a 4-h immersion at 80 °C. A 200-nm-thick Ni Schottky metal was patterned, evaporated, and lifted off to form circular anode pads. A 700-nm-thick SiO₂ layer was then deposited by plasmaenhanced chemical vapor deposition (PECVD), patterned, and etched with CHF₃/Ar reactive ion etching (RIE). After photoresist stripping, the circular SiO₂ layer on top of Ni served as an etching mask for GaN mesa etching. A 1.2- μ m-deep GaN mesa etching was performed with BCl₃/Cl₂ RIE, which additionally partially etched the SiO₂ mask layer. The remainder of the SiO₂ mask layer was then dissolved by immersion into a 6:1 buffered oxide etchant (BOE). A Ti/Al/Ni/Au (20/120/40/50 nm) stack was evaporated and lifted off to form ring shape ohmic contacts with n^+ -GaN without annealing. A cross-sectional schematic of the circular diodes is shown in Fig. 1(a). Fig. 1(b) illustrates that the built-in potential and the depletion width for camel diodes are expected to be higher than those of Schottky diodes and therefore reduce the reverse bias leakage current.

B. Static Characteristics

The reverse leakage current plays a crucial role in varactor performance. Paths of the diode leakage can be categorized into bulk (including junction) and sidewall (surface) leakages.



Fig. 2. Circular diodes and their *I*–V, *CV*, and J_{leak} –*V* characteristics. (a) Images of circular diodes and schematic of the leakage current paths for bulk leakage and sidewall leakage. (b) Comparison of J_{leak} – V_{rev} of GaN/QST camel diodes and GaN/GaN Schottky diodes. (c) Average current density dependence with anode radii of 95 μ m (six devices), 140 μ m (six devices), 185 μ m (four devices), 230 μ m (three devices) at –20 V. The error bars represent standard deviation. (d) *I*–V turn-on characteristics of a Schottky diode and 11 camel diodes with R = 100, 120, 140, and 160 μ m on QST substrate. (e) Measured CV_{rev} characteristics of ten camel diodes with R = 100, 120, 140, and 160 μ m on QST substrate normalized with diode area. (f) Plot of $1/C^2$ versus V_{rev} and the extracted N_{eff} and of ten camel diodes with R = 100, 120, 140, and 160 μ m on QST substrate normalized with diode contact area.

We fabricated circular diodes with different diameters to investigate whether bulk or surface leakage currents were dominant [see Fig. 2(a)] [32]. A leakage current density that is dependent on the area of the diode, i.e., exhibits parabolic dependence on the radius of the diode contact, indicates that volumetric or bulk leakage is dominant. A leakage current density that is linearly proportional to the radius of the diode contact indicates that surface leakage current is dominant. In Fig. 2(b), we compare the leakage and breakdown characteristics of circular diodes on GaN/QST substrate (1-µm n⁻-GaN, $N_{\rm eff} = 1.5 \times 10^{17} {\rm cm}^{-3}$) and that of a Schottky diode on freestanding GaN substrate (1- μ m n⁻-GaN, $N_{\rm eff}$ = 3 × 10^{17} cm⁻³). The reverse breakdown characteristics of 24 camel diodes and five Schottky diodes were measured with a Keithley 2410 source meter. Camel diodes, with their higher built-in potential than Schottky diodes, were characterized with significantly lower leakage currents and significantly higher breakdown voltages than Schottky diodes. For the camel diodes, the leakage current density did not significantly change with the radius of the diode contact [see Fig. 2(c)], indicating a dominant bulk leakage current and that the optimized RIE etching process does not lead to appreciable surface current leakage. The forward I-V and reverse CV characteristics were measured with a B1500 parameter analyzer. The turn-on voltages were around 0.5 V for Schottky diodes and

around 4.5 V for diodes with p^+ surface layers [see Fig. 2(d)], which further supports their superior leakage and breakdown behavior. The ohmic contact to the n⁺-GaN diode body was not annealed to avoid possible degradation of the Schottky contact. As a result, this contact may contribute to a series resistance, which in turn leads to a higher turn-on voltage than the GaN bandgap of 3.4 V. This however does not compromise the varactor operation, which functions in reverse bias. The ohmic contact to the n⁺-GaN is used to apply a reverse dc bias to the diodes and must be connected to a high value bias resistor to block any RF leakage. Therefore, the lowresistance ohmic contact is not needed for this contact. The CV characteristics of the varactors with p^+ surface layers were measured as a function of reverse bias [see Fig. 2(e)]. The ten devices that were measured exhibited uniform characteristics in the voltage range of 0 to -40 V, with a C_{0V}/C_{-40V} of approximately 3.5. Fig. 2(f) shows a plot of $1/C^2$ as a function of reverse bias. The n⁻-GaN drift layer effective carrier concentration ($N_{\rm eff}$) of 1.5 \times 10¹⁷ \pm 7 \times 10¹⁵ cm⁻³ was extracted from the slope of $1/C^2 - V$ curve according to

$$N_{\rm eff} = \frac{2}{q\gamma_0\gamma_s} \left[-\frac{1}{d(1/C^2)/dV} \right] \tag{1}$$

where ε_0 is the permittivity of free space, ε_s of 10 is the dielectric constant of GaN, and *C* is the capacitance that arises from depletion in the n⁻-GaN [33]. Overall, the circular diodes exhibited robust static *I*–*V* and *CV* characteristics.

III. MULTI-FIN ANTI-SERIES DIODES A. Device Structure and Fabrication Process

Fig. 3 shows the fabrication process flow of the GaN multi-Fin anti-series varactor diodes. The anti-series configuration sustains high varactor linearity, and the multi-Fin structure reduces the series resistance path between the diodes and therefore maintains high Q values. The first steps in the fabrication process are identical to the circular diode fabrication process steps up to the GaN etching step. The only significant differences for the multi-Fin varactors were the thickness and composition of the Fin contact metal lines, which were significantly thicker and made of Ni/Au/Ti/Au (40/100/100/1200 nm), as shown in Fig. 3(a). The thicker metal lines atop the Fins reduce the current spreading resistance from the Ni Schottky contact to the p⁺-GaN top layer of the epitaxial structure of the varactor diode. The samples were then immersed in 40 °C, 25% tetramethylammonium hydroxide (TMAH) for 10 min to smoothen the plasma damaged sidewalls that were specifically aligned parallel to the m-plane that we found to be smoother than those aligned to a-plane with the same process. Immediately after rinse and dry, the sample was coated with SiN_x/SiO_2 (120/4500 nm) by PECVD and was patterned to define varactor isolation by deep GaN RIE etching of 12 μ m with a BCl₃/Cl₂ plasma to eliminate parasitic effects from conductive GaN. An RIE plasma etch with CHF₃/Ar gas followed by a BOE oxide etch was performed to remove the remaining dielectric layers atop n⁺-GaN. An ohmic contact metal stack on n⁺-GaN consisted of Ti/Al/Ni/Au (20/120/40/50 nm) was evaporated and lifted off [see Fig. 3(b)]. After mesa-isolation and to implement ground-source-ground (GSG) pads for RF characterization, a



Fig. 3. Fabrication process flow of the anti-series multi-Fin varactor diodes with interdigitated structure. (a) Definition of Schottky metal Ni/Au and etch GaN Fin with RIE. (b) Smoothening and passivation of GaN sidewalls by TMAH treatment and SiN_x deposition. Deep etching of GaN with RIE for varactor isolation and deposition of Ti/Al/Ni/Au Ohmic contacts atop n^+ GaN. (c) Patterning and curing of photo-definable PI and the formation of vias for metallization to connect to the Schottky/ohmic contacts. (d) Definition of GSG metallization with Ti/Au layers and of snake-shaped Ti resistor followed by ALD Al₂O₃ passivation. XeF₂ isotropic Si etch to remove the underlying Si layer below the diodes.



Fig. 4. Cross-sectional view of the bonding layers and the XeF₂ anisotropic silicon etching process. (a) Cross-sectional SEM of our initial multi-Fin diodes showing PI encapsulation as well as the intermediate layers between GaN and the polycrystalline AIN substrate. (b) Illustration of the varactor release method with XeF₂ flow through the PI vias and lateral etching of the silicon conductive plates. (c) Top view image of a sample exposed to the XeF₂ process.

polymer fill-in step was performed. We used HD-4104 photodefinable polyimide (PI) to encapsulate the entire device and expose only the Schottky and ohmic metal contacts on the multi-Fin varactors [see Fig. 3(c)]. Ti/Au (100/1200 nm) GSG pads and Ti (40 nm) resistors were defined followed by the deposition of Al₂O₃ (25 nm) passivation layer with atomic layer deposition (ALD). The sample was then patterned with photoresist and underwent a XeF₂ anisotropic silicon etching to remove the silicon nucleation layer in between GaN and AlN substrate. The final structure prior to being released from the QST substrate is illustrated in Fig. 3(d).

Fig. 4(a) shows a cross-sectional image of our very first device without the XeF₂ release process. Between GaN and poly-AlN, there are AlGaN/AlN buffer layers for GaN growth on a thin silicon layer as well as additional bonding layers that include SiO₂, SiN_x, and silicon. The effect of XeF₂ is delineated in Fig. 4(b), where the XeF₂ gas flows through via holes in the PI layer and laterally etches the silicon layer present at the surface of the poly-AlN substrate. Once this silicon layer is fully etched, the GaN varactors embedded in polyimide levitate from the surface of the substrate. This freestanding structure does not naturally separate from the substrate and remains hinged in the non-XeF₂ etched regions.



Fig. 5. Experimental implications of center parasitic capacitance originated from the silicon plate. (a) Comparison of two-port S_{11} and S_{21} for a device before and after XeF₂ process. (b) Test structure with n-type ohmic contact at signal pad and open at ground side. (c) One port S_{11} measurement showing that there is lower capacitance after the XeF₂ process. (d) Capacitance extracted by EM S_{11} simulation for the cases of with and without a buried conductor representing the silicon plate on AIN.

The top view optical image after XeF_2 etching process is shown in Fig. 4(c), where the contrast allows one to discern levitated and hinged parts of the structures on the substrate.

The conductive silicon sheet under the varactors can lead to additional stray capacitance that compromises their RF behavior. The XeF2 etching process is necessary to reduce the impact of this center parasitic capacitance, which is supported by both experimental results and by computational analysis. In a two-port S-parameter measurement, the S_{11} curve should lie inside the 50- Ω circle of the Smith chart, as expected for an ideal resistor placed in series with a capacitor because the total resistance is supposed to be higher than 50 Ω . However, a device not processed with the silicon removal by XeF₂ exhibits a signature of high capacitance to ground; S_{11} does not stay within 50- Ω circle throughout the 100-MHz-26.5-GHz frequency range. On the contrary, after the XeF₂ process, S_{11} lies within the 50- Ω circle, as shown in Fig. 5(a). To further support this analysis, a one port test structure that has signal pad (input port) connecting to n⁺-GaN and ground



Fig. 6. Cross-sectional SEM images of the interdigitated diodes and optical images of one- and two-port devices. (a) Close view of Fins illustrating the structure of the diodes. (b) Another wider field of view SEM showing the device levitation after XeF₂ etch step. (c) Schematic of diodes anti-series connected. (d) One-port devices with GSG pads and a Ti resistor. (e) Two-port devices with GSG pads and a Ti resistor. The scale bars for the optical images are 60 μ m.

pad atop PI without connecting to n⁺-GaN was fabricated [see Fig. 5(b)]. The capacitance extracted from S_{11} before and after XeF₂ etching process is plotted in Fig. 5(c). The reduction of capacitance indicates that the center capacitance below varactors can be obviated by eliminating the conductive silicon sheet. A qualitative analysis of the effect of this extra silicon sheet was investigated with ADS Momentum electromagnetic simulation. The simulation results shown in Fig. 5(d) indicated that capacitance calculated with buried conductive layer is much higher than that without a conductive layer underneath, in agreement with those experimental results of Fig. 5(c).

The final devices that were released from the QST substrate are shown in Fig. 6. Fig. 6(a) displays a cross-sectional SEM view of the final structure, including Schottky metal, n⁻⁻ GaN, n⁺-GaN. Both the Schottky metal thickness and the GaN etch depth exceeded 1 μ m. The thick Schottky metal aims to retain low series resistance caused by the metal itself, and at least 1- μ m deep GaN trenches confine the signal path in the anti-series configuration to be n⁻-GaN/n⁺-GaN from one Fin capacitor the n⁺ GaN/n⁻ GaN of the second antiseries capacitor. One can also notice from Fig. 6(a) that GaN sidewalls are passivated by SiN_r/SiO_2 dielectric layers. SiN_r is too thin to be discerned in the image. The device levitation after XeF₂ etching can be seen in the zoom-out cross-sectional view of Fig. 6(b), where the black contrast at the bottom of the image indicates the absence of any underlying layer. Antiseries [see Fig. 6(c)] diodes prepared for one-port S-parameter measurements to characterize R_s , C_s , and quality factor (Q) and two-port devices for two-tone linearity measurements are shown in Fig. 6(d) and (e), respectively.

B. Static Characteristics

The multi-Fin diodes with different fin lengths (20 and 40 μ m) and different numbers of fins (5 and 10) exhibited uniform *CV* characteristics for 22 devices measured in the voltage range of 0 to -40 V, as shown in Fig. 7(a). The reverse leakage current density and breakdown characteristics of nonleaky circular and multi-Fin diodes are plotted in Fig. 7(b). In general, we found that the yield of 12 out of 22 multi-Fin diodes. However, for devices that



Fig. 7. DC CV_{rev} and J_{leak} . V_{rev} characteristics of multi-Fin varactors. (a) Normalized CV curves of 22 multi-Fin diodes (not measured under anti-series configuration). Number of Finrs and Fin length in four structures are 5 Fins/20 μ m, 5 Fins/40 μ m, 10 Fins/20 μ m, 10 Fins/40 μ m, corresponding to as-designed single diode area 6.05 × 10⁻⁶, 8.35 × 10⁻⁶, 1.28 × 10⁻⁵, and 1.74 × 10⁻⁵ cm². (b) Comparison of reverse bias dependence of leakage current density between 19 circular diodes and 12 multi-Fin diodes with relative low leakage current. For devices with comparable low leakage current density, circular diodes have higher breakdown voltage.



Fig. 8. S-parameter measurement results and extractions of capacitance and series resistance for 5 Fins/20 μ m and 5 Fins/40 μ m devices. (a) 5 Fins/20 μ m S₁₁ plot in Smith chart for 0- and -25-V bias conditions. (b) 5 Fins/40 μ m S₁₁ plot in Smith chart for 0- and -25-V bias conditions. (c) Capacitance values for different devices and bias conditions calculated using $Im(Z_{in})$. (d) Series resistance values of different devices and bias conditions extracted from $Re(Z_{in})$.

were not leaky, the current density in both configurations was comparable. Additionally, those nonleaky multi-Fin diodes exhibited lower breakdown voltage than the circular diodes attributed to the enlarged electric field at sharp edges in the higher surface area of the multi-Fin structures than that of circular structures. The highest breakdown voltage for the multi-Fin diodes was -146 V, which was lower than -196 V of the circular diodes. This lower breakdown voltage for multi-Fin diodes does not preclude excellent varactor RF performance as will be discussed next.

C. One-Port S-Parameter Characteristics

The one-port *S*-parameter measurements with two structures of anti-series multi-Fin diodes of 5 Fins/20 μ m and 5 Fins/40 μ m were measured and are presented in Fig. 8. These devices have 3- μ m Fin width and 2- μ m spacing. The *S*₁₁ measured with an Agilent N5242A network analyzer from 100 MHz to 26.5 GHz under different reverse bias conditions provided by an Agilent E3631A dc power supply is plotted in Smith charts in Fig. 8(a) and (b). The modulation of the depletion width in the diodes with reverse dc bias can be confirmed with the bias-dependent traces in the Smith chart figures. The blue curves represent S_{11} under zero bias with a larger capacitance indicating smaller depletion width. The red curves represent a -25-V bias and smaller capacitance corresponding to larger depletion width. The series capacitance expressed as

$$C_s = -\frac{1}{2\pi f Im(Z_{\rm in})} \tag{2}$$

and the series resistance expressed as

$$R_s = Re(Z_{\rm in}) \tag{3}$$

can be extracted from the input impedance that is computed from the *S*-parameter measurement according to

$$Z_{\rm in} = Z_O \frac{(1+S11)}{(1-S11)} \tag{4}$$

where f is the frequency and $Z_o = 50 \ \Omega$. Fig. 8(c) illustrates the extracted C_s of different devices under 0 and -25-V bias. The capacitance curves were characterized by a convex shape due to the higher contribution of the parasitic inductance to input impedance at high frequencies above 10 GHz. The imaginary part of input impedance can be expressed as

$$Im(Z_{\rm in}) = -\frac{1}{2\pi fC} + 2\pi fL \tag{5}$$

where *C* and *L* symbolize the quantities associated with each measurement. From the measurement analysis, we determine an extracted capacitance, C_s , and estimated series inductance, L_s . In order to understand the relationship between C_s , L_s , and Z_{in} , we introduce the estimated capacitance, C_{est} , which represents the ideal capacitance of the diode, C_{est} , assumed to be frequency independent. Moreover, to obviate nonideal effects at the low-frequency regime and the inductance contributions at high-frequency regime, we determined C_{est} values by averaging extracted C_s values in the frequency range of 4–6 GHz and calculated L_s according to

$$L_s = \frac{1}{2\pi f} \left(\frac{1}{2\pi f C_{\text{est}}} + Im(Z_{\text{in}}) \right). \tag{6}$$

Here, the inductance estimation was expected to be most accurate when the frequency was 26.5 GHz, the highest frequency in our measurements. C_{est} values for 5 Fins/20 μ m at 0 and -25 V and for 5 Fins/40 μ m at 0 and -25 V were 175, 90, 233, and 124 fF, respectively. L_s calculated at 26.5 GHz for 5 Fins/20 μ m at 0 and -25 V and for 5 Fins/40 μ m at 0 and -25 V are 80, 80, 89, and 89 pH, respectively. L_s does not scale much with varactor finger length since the metal trace connected to one diode and ground [see Fig. 6(d)] also contributes to series inductance importantly. Fig. 8(d) shows the extracted R_s calculated by $R_s = Re(Z_{in})$, where the frequency-dependent resistance is more prominent at the lower frequencies. With these calculations, we can now compute the quality factors, which are critical figures of merit of varactors and are calculated according to

$$Q = \frac{Im(Z_{\rm in})}{Re(Z_{\rm in})} \tag{7}$$

as plotted in Fig. 9(a). For both measured devices, the calculated Q values as a function of frequency at -25-V bias



Fig. 9. Frequency dependence of quality factor (*Q*) in two devices plotted by two methods. (a) *Q* versus frequency plot calculated using the measured $Im(Z_{in})/Re(Z_{in})$. (b) $Q_{\text{extrapolated}}$ versus frequency plot by estimating the capacitance and the series resistance and by excluding the series inductance and nonideal effects caused by measurement as described in the text.

TABLE ISERIES RESISTANCE CONTRIBUTION FOR R_M , R_{n-} , and R_{n+} to R_{TOT}

	R _M /R _{tot} (%)	Rn-/Rtot (%)	R _{n+} /R _{tot} (%)
μ _{n-GaN} 500 cm ² /V-s	2.4	52.4	45.2
μ _{n-GaN} 300 cm ² /V-s	1.9	62.8	35.3

voltage are higher than those calculated for a 0-V bias. For a given bias, the Q curves of both devices closely overlap indicating that doubling the Fin length from 20 to 40 μ m does not contribute to an increase in the series resistance that compromises Q. The measured Q values at 2 GHz for 5 Fins/20 μ m at 0 and -25 V and for 5 Fins/40 μ m at 0 and -25 V were 27, 34, 24, and 32, respectively. At 10 GHz, they were 11, 20, 11, and 20, respectively. The plot of O versus frequency in Fig. 9(a) does not exhibit an ideal inverse relationship with the frequency below 5 GHz mainly due to the frequency-dependent R_s in our extractions. There are a few possible causes to this nonideality including, but not limited to, parasitic components not understood in these diodes, inaccurate calibration, or phase/magnitude inaccuracy of the Agilent N5242A network analyzer. Another possible parasitic component is the formation of a Ni/nonfully depleted p-GaN junction, which could produce large series contact resistance coupled with capacitive components. As-measured multi-Fin diodes exhibited an overall higher series resistance and a lower quality factor than expected at low frequency. To better predict these values and exclude the low-frequency nonidealities, we used C_{est} discussed before and $R_{\rm st}$ (R_s extracted at 26.5 GHz) to extrapolate Q for the entire frequency range. The extrapolated quality factor

$$Q_{\text{extrapolated}} = \frac{1}{2\pi f C_{\text{est}} R_{\text{est}}}$$
(8)

is plotted in Fig. 9(b) as a function of frequency. This reveals significantly higher Q values in the sub-5-GHz low-frequency regime than those complicated by the measurement nonidealities and illustrates the potential of our multi-Fin diodes for high-performance varactors. The $Q_{\text{extrapolated}}$ values at 2 GHz for 5 Fins/20 μ m at 0 and -25 V and for 5 Fins/40 μ m at 0 and -25 V were 73, 163, 84, and 181, respectively. At 10 GHz, they are 14, 32, 16, and 36, respectively.

Aside from anomaly in the behavior of the series resistance at low frequency, the extracted series resistance at high frequency appears to be the main limitation in this set of

Technology	SS Tuning	Punch-Through	Breakdown (V)	\mathbf{Q}_{\min}	Qmax	VFOM
SiC [34, @ 2GHz]	5.6/1	15	40	8	45	1100
GaAs [36, @ 2GHz]	9:1	15	28	22	150	5280
GaN [18, @ 1GHz]	5:1	N.A.	120	N.A.	>35	<16800
SiC [35, @ 2GHz]	6:1	60	>150	20	160	12000
This Work [@ 2GHz]	6.4:1	138 (expected)	Circular: 196 Multi-Fin : 146	>30 (measured) >70 (extrapolated)	N.A. >420	44700

TABLE II COMPARISON OF KEY FOMS FOR MICROWAVE POWER VARACTORS



Fig. 10. Evaluation of the large signal tuning capability of the GaN diode. (a) Schematic illustrating the method for determining C_{max} and C_{min} . (b) Comparison of power varactor technologies for capacitance tuning range versus superimposed signal voltage amplitude.

varactor diodes. Specifically, in the optimal operating regime with a varactor impedance of 50 Ω , the operating frequency is approximately 3 GHz for a 1-pF varactor capacitance. At this frequency, the extrapolated Q is 56 at zero bias, which is not optimal for various applications. To explore the possible origins of the series resistance and deduce possible mitigation strategies, we used ADS Momentum EM simulation. The Schottky metal resistance (R_M) , the nondepleted n⁻-GaN resistance (R_{n-}) , and the n⁺-GaN resistance (R_{n+}) contributions were calculated for two cases for the n⁻-GaN mobility of 1) 300 and 2) 500 cm²/V-s. Based on measurements for test device structures, we used an empirical conductivity of $1.4 \times$ 10^7 S/m for the Schottky metal and an empirical resistivity of 8100 S/m for the n⁺-GaN in the simulation setup. Table I shows the ratio of the three resistance components, R_M , R_{n-1} , and R_{n+} to the total series resistance, R_{tot} , where both R_{n-} and R_{n+} appear to dominate R_{tot} . Therefore, to further improve Q, both the mobility of the n⁻-GaN layer and the conductivity of the n⁺-GaN need to increase in the epitaxial structures that form the varactor diodes.

IV. BENCHMARK PROJECTION

To better understand the potential of GaN-based camel diodes for power varactor applications, we compare this work with other varactor technologies using different figures of merit and criteria. For a power varactor, it is crucial to provide a wide tuning range with a high input power. When the input power is high, we need to operate the varactors with a negative bias voltage to avoid driving the varactor diode to the forward bias regime with the ac swing. This results in a maximum operating capacitance (C_{max}) that is smaller than the highest achievable capacitance at 0 V. Additionally, we need to operate the varactor at a minimum operating capacitance, so that the signal voltage amplitude added to the reverse bias does not lead to reverse voltage breakdown.



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Fig. 11. Comparison of different varactor technologies for their cutoff frequency versus small signal tuning range.

A schematic of C_{max} and C_{min} definitions can be found in Fig. 10(a). Using these definitions, we computed a small signal tuning ratio of 5 in the bias range of 0 to -100 V, and the highest dc voltage we were able to apply in our CV characterization setup with small signal voltage amplitude of 100 mV. We note that a small signal tuning ratio of 6.4 is expected in the bias range of 0 to -138 V, where punchthrough occurs for the 1- μ m drift layer. Fig. 10(b) exhibits effective tuning ranges as a function of superimposed signal voltage amplitudes for different power varactor technologies. Our diodes demonstrate a high tuning range throughout the whole voltage amplitude span. Table II summarizes key metrics that evaluate the performances of power varactors. The varactor figure of merit (VFOM) accounts for tuning range, for Q, and for power handling at the desired signal frequency of operation and is determined as follows:

$$VFOM = (TR - 1) f V_{max} Q_{min}$$
(9)

where TR is the tuning ratio, f is the frequency of operation, $V_{\rm max}$ is the punchthrough voltage, and $Q_{\rm min}$ is the quality factor without applied reverse voltage bias. Our varactors exhibited high tuning ratio with a wide range of voltage amplitudes, higher punchthrough voltages, and highest breakdown voltages with superior quality factors, which result in better VFOM than the existing SiC [34], [35], GaAs [36], and GaN [18] microwave power varactors, as shown in Table II. The GaN camel diode varactors offer concurrent high cutoff frequency and high tuning range compared to other highpower varactors technologies. This is illustrated in Fig. 11, which plots the cutoff frequency as a function of small signal tuning range for a variety of varactor technologies including the projected valued for our GaN camel diode like varactors [19], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44]. In conclusion, GaN-based camel diode varactors are promising to facilitate more RF adaptive circuit applications, where high power signals are transmitted.

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