A Comprehensive Large Signal, Small Signal, and Noise Model for IGZO Thin Film Transistor Circuits

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***Abstract*— We report a new physics-based model for dual-gate amorphous-indium gallium zinc oxide (a-IGZO) thin film transistors (TFTs) which we developed and fine-tuned through experimental implementation and benchtop characterization. We fabricated and characterized a variety of test patterns, including a-IGZO TFTs with varying gate widths (100–1000 μm) and channel lengths (5–50 μm), transmission-line-measurement patterns and ground–signal–ground (GSG) radio frequency (RF) patterns. We modeled the contact resistance as a function of bias, channel area, and temperature, and captured all operating regimes, used physics-based modeling adjusted for empirical data to capture the TFT characteristics including ambipolar subthreshold currents, graded interbias-regime current changes, threshold and flat-band voltages, the interface trap density, the gate leakage currents, the noise, and the relevant small signal parameters. To design high-precision circuits for biosensing, we validated the dc, small signal, and noise characteristics of the model. We simulated and fabricated a two-stage common source amplifier circuit with a common drain output buffer and compared the measured and simulated gain and phase performance, finding an excellent fit over a frequency range spanning 10 kHz–10 MHz.**

***Index Terms*— Circuit model, flexible electronics, indium gallium zinc oxide (IGZO), thin film transistors (TFTs).**

I. Introduction

AMORPHOUS indium gallium zinc oxide (a-IGZO) thin film transistors (TFTs) were first reported in 2004 as a promising alternative to amorphous Si (a-Si:H) TFTs, and have subsequently evolved over the last two decades to dominate the driving circuits in modern displays [1], [2], [3]. a-IGZO thin films can be deposited at relatively low temperatures without compromising charge carrier mobility and are thus favored for applications with a low thermal budget [4], [5], [6]. Recent advances in the a-IGZO TFT fabrication technology have allowed the development of high-speed circuits for applications in displays, flexible devices, and electronics, paving the way for the large-scale integration of a-IGZO TFTs in active acquisition circuits built on flexible substrates for use in biomedical applications such as neural probes and wearable sensors [7], [8], [9], [10].

To exploit the unique properties of a-IGZO TFTs for designing high-speed and high-precision signal processing with integrated circuits on thin-film polymer substrates, the systematic development of a unified physics-based model that can accurately predict the device performance in all operational regimes is needed. Developing such a unified model requires evaluating device parameters over multiple channel areas, at different device temperatures and in different operating regimes to empirically extract the intrinsic device parameters [11], [12], [13], [14]. Understanding the dependencies of these parameters facilitates greater flexibility in the design of circuits which can be implemented for low-noise, high-speed, and high-precision signal processing [15], [16], [17]. Important device properties, such as the threshold voltage, channel mobility, and contact resistance can be controlled by modifying the fabrication parameters, including but not limited to the oxygen partial pressure during deposition, the film thickness and the source/drain contact material. Therefore, it is critical to develop a physics-based TFT device model while clearly disseminating the steps needed for the empirical reproduction of a-IGZO TFT characteristics for any given material and device processing conditions [18], [19], [20].

In this work, we demonstrate a-IGZO TFTs on flexible films that exhibit a field-effect mobility of $\sim$15 cm^2/V·s, an ON/OFF current ratio exceeding 10^9, low gate-leakage currents less than 1 nA, high cutoff frequencies greater than 50 MHz, and Hooge's coefficient of noise of $\sim$0.005. We performed parametric studies to develop a more complete model for a-IGZO TFTs that captures the subthreshold, linear, and saturation operating regimes, the ac characteristics, leakage currents, noise currents, and contact resistance and we validated the accuracy of the model by illustrating excellent agreement

Manuscript received 3 April 2023; accepted 5 June 2023. This work was supported in part by the National Science Foundation under Grant CMMI-1728497 and Grant ECCS-2114482; in part by the National Institutes of Health under Grant NIBIB DP2-EB029757; in part by the Brain Research Through Advancing Innovative Neurotechnologies (BRAIN) Initiative under Grant R01NS123655-01 and Grant UG3NS123723-01; and in part by the Center for Design Enabled Nanofabrication (C-DEN) sponsored by ASML, Cadence, Zeiss, Intel, KLA Tencor, and Mentor Graphics. The review of this article was arranged by Editor B. Iñiguez. *(Corresponding author: Shadi A. Dayeh.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2023.3284803.

Digital Object Identifier 10.1109/TED.2023.3284803

between the performance of experimentally realized a-IGZO TFT circuits and simulated circuits.

II. Proposed Model

Early investigations into device and circuit models for TFTs focused on a-Si TFTs [21], [22], [23], [24]. In recent years, with the rapid developments made in fabrication techniques for a-IGZO TFTs, device models for a-IGZO TFTs have been developed by modifying existing a-Si circuit models [25], [26]. An a-IGZO specific physics-based device model that can capture the bias-dependent and parameter-dependent changes in the contact resistance, gate leakage current, and subthreshold leakage current, and the device noise current is currently lacking. Recent advances in thin film fabrication have paved the way for high-speed circuits using TFTs [27]. Further translational application of TFTs in high-speed, high-precision circuits, especially for biosensing applications mandates the development of an accurate device model for novel circuit designs.

The foundational model for a-Si TFTs was introduced by Shur et al. [24] at the Rensselaer Polytechnic Institute (RPI). Our proposed model is based on the RPI TFT model, by developing parametric equations for device parameters including the contact resistance, threshold voltage, mobility, and leakage current. The model investigates the underlying physical mechanism for each process but recognizing that variations arise due to differences in the fabrication conditions, device structure, and design, including but not limited to the choice of the gate dielectric, contact metal at the source and drain, and the electronic properties of the channel, which can be controlled by the thickness of the deposited IGZO film, the amount of O_2 present in the deposition chamber and the annealing temperature of the IGZO film. While the device parameters used in our model are calculated empirically, it is important from a circuit design perspective to understand the physical basis of each parameter to ensure that the model remains broadly applicable regardless of changes to the process conditions. The physically justified equations used in the model ensure that the circuit designer has control over the parameters that need to be optimized to achieve ideal performance, independent of the fabrication conditions used.

To ensure broad applicability, the model uses empirical data from test devices of different channel lengths and widths, as well as dedicated transfer length measurement patterns to extract the inherent dependencies of each device parameter on the device geometry, while outlining steps that can be followed to calculate each parameter that is introduced in the model. The proposed model uses empirical data collected from devices built on flexible substrates and fits them into physics-based equations representing processes known to be active in TFTs. The device model was written using the Verilog-A analog programming language. The circuit simulations were performed using the Cadence Spectre SPICE-class simulator, which supports Verilog-A for device modeling. Verilog-A is one of the most popular hardware description languages used for MOSFET and TFT models. It is a procedural language similar to C, and it allows simple constructs for device behavior. This essentially allows us to decouple the model function from the simulator being used and allows us to investigate model functioning independent of the type of analysis being run [28]. The a-IGZO TFTs that we studied are composed of different channel lengths (L = 5, 7.5, 10, 12.5, 15, 17.5, 20, and 50 μm) and widths (W = 100, 200, 500, and 1000 μm) with example devices shown in Fig. 1(a) and output and transfer curves shown in Fig. 1(b)–(e). Fig. 1(d) and (e) illustrates that the TFT dimensions play a significant role in determining critical device parameters such as the threshold voltage, off current and subthreshold slope. The device equations and corresponding parameter values used for these simulations are summarized in Table I. In the next section, we discuss the experimental paradigms that we used to extract the model parameters.

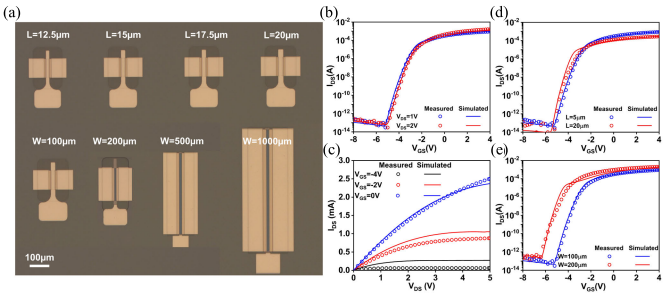

Fig. 1. (a) Optical microscope image of the test device structures of different channel lengths for a W = 100-μm device and different channel widths for an L = 5 μm device. (b), (d), and (e) Measured and simulated transfer as a function of drain bias, channel length, and width. (c) Measured and simulated output curves.

A. Contact Resistance

The Ti/Au contacts at the source and drain form an ohmic contact [29], [30]. In the ON-state, contact resistance can account for up to one-third of the total observed TFT resistance [31], [32]. If not accounted for properly, this can lead to significant errors in determining critical device parameters [33], [34]. To extract the contact resistance, R_{contact}, as a function L, W, V_{GS}, and T, we use both gated and ungated linear transmission line measurement (TLM) patterns [Fig. 2(a)] [35], [36]. The a-IGZO TFTs reported in this work are depletion mode devices, and are readily "on" at a zero gate bias, exhibiting linear I–V characteristics without the application of a gate bias.

The inverse slope of I–V measurements provides a measure of the total channel resistance consisting of the contact resistances at the source, R_{S}, and drain, R_{D}, and the total channel resistance, R_{ch}. For a device with a long metal contact overlap over the channel, R_{contact} can be expressed as $R_{\text{S}} = R_{\text{D}} = R_{\text{contact}}/2$ and $R_{\text{ch}} = R_{\text{sh}} \times L_T/W$, where R_{sh} is the sheet resistance of the channel, and L_T is the contact transfer length [37].

R_{contact} varies inversely with the width of the contact [Fig. 2(b) and (d)] and decays exponentially with V_{GS} [Fig. 2(c)] due to a decrease in the Schottky barrier width at the source/drain (S/D) contacts [33]. Furthermore, we found that the contact resistance increases exponentially with temperature [Fig. 2(e)] due to the diffusion of mobile carriers into the

TABLE I
PARAMETERS FOR THE DEVELOPED MODEL

Group	Parameter	Description	Value	Unit
Process Parameters	L	Channel Length	5, 7.5, 10, 12.5, 15, 17.5, 20	µm
	W	Device Width	100, 200, 500, 1000	µm
	C_{ox}	Oxide Capacitance	5.067×10^{-3}	F/m^2
	t_{ox}	Oxide Dielectric Thickness	25	nm
	L_{ov}	Overlap of Gate with Source/ Drain	5	µm
	RT	Room Temperature	22	°C
Contact Resistance	ρ_c	Contact Resistivity	0.0212	Ωm
	k_1	Dependence Parameter for Contact Resistance Variation with Gate Bias	0.641	V^{-1}
	k_2	Exponential Dependence Parameter for Contact Resistance Variation with Temperature	0.051	°C^{-1}
On Current	V_{th0}	Threshold Voltage Parameter	-4.17	V
	A_t	Parameter for the Variation of Threshold Voltage with the Drain Bias	0.1063	µmV^{-1}
	B_t	Parameter for the Variation of Threshold Voltage with the Channel Length	3.822	µmV
	K_{Vth}	Parameter for the Variation of the Threshold Voltage with Temperature	0.0224	VK^{-1}
	μ_0	Bulk Mobility	11.3	cm^2/Vs
	k_3	Parameter for the Variation of the Mobility with Channel Length	2200	cm/Vs
	k_4	Parameter for the Variation of the Mobility with Temperature	0.067	cm^2/°C Vs
	γ	Field Effect Mobility Parameter	0.0476	1
	λ	Channel Length Modulation Parameter	0.0421	V^{-1}
	α_{sat0}	Saturation Modulation Parameter	0.268	1
	$k_{\alpha sat}$	Parameter for the Variation of the Saturation Modulation with Channel Length	0.0215	1
	$k_{\alpha T}$	Parameter for the Variation of the Saturation Modulation with Temperature	0.0034	°C^{-1}
Sub-threshold Current	I_{off}	Sub-threshold current at Flat Band Gate Voltage	813.1	nA
	η_i	Sub-threshold Ideality Factor	3.7	1

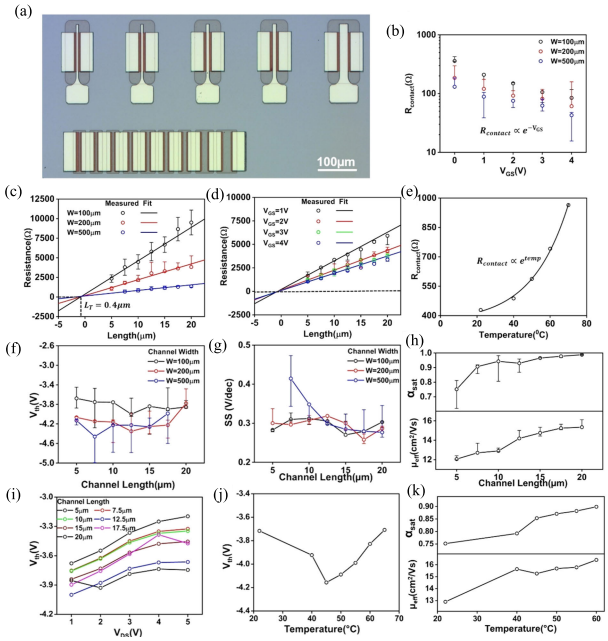

Fig. 2. (a) Optical microscope image of the test devices and TLM patterns. (b) Extracted contact resistance as a function of gate bias for different device widths. Measured and fit plots of the total resistance as a function of the channel length for TLM patterns with different (c) device widths as a function of the channel length (L) and (d) for a fixed device width of 100 μm and different gate bias voltages as a function of L. (e) Extracted contact resistance as a function of temperature for 100-μm-wide devices. The dependence of threshold voltage on (f) channel length and (i) drain bias (for 100-μm-wide devices). (g) SS of the device as a function of the channel length for multiple device widths. (j) Variation of threshold voltage with temperature. The variation of the mobility and saturation pinning parameter with (h) channel length and (k) temperature.

oxygen vacancies in the IGZO film. Charge carrier termination in the oxygen vacancies decreases the number of available defect states in the channel and consequently increases the barrier height and the contact resistance [38]. Considering these effects, we developed a general expression for the contact resistance as follows:

$$R_{\text{contact}} = \frac{\rho_c}{W} e^{-k_1 V_{\text{GS}}} e^{k_2 (T-22)} \tag{1}$$

where k_1 and k_2 are determined empirically from the fits shown in Fig. 2(b) and (e), respectively, and are shown in Table I.

B. DC Characteristics

The measured dc current from the drain comprises the subthreshold current ($I_{\text{sub-vt}}$), the above threshold drift current (I_{ON}), the drain–to-source leakage current ($I_{\text{D,leak}}$), and the noise current in the channel (I_{noise}). The overall drain current is represented as follows:

$$I_{\text{DS}} = f(I_{\text{ON}}, I_{\text{sub-vt}}) + I_{\text{noise}} + I_{\text{D,leak}} \tag{2}$$

where $f(I_{\text{ON}}, I_{\text{sub-vt}})$ accounts for the transition from the sub-threshold current ($I_{\text{sub-vt}}$) to the above-threshold drift current according to Matthiessen's rule [39] as follows:

$$f(I_{\text{ON}}, I_{\text{sub-vt}}) = \frac{I_{\text{ON}} \times I_{\text{sub-vt}}}{I_{\text{ON}} + I_{\text{sub-vt}}}. \tag{3}$$

In the deep subthreshold regime ($V_{\text{GS}} \ll V_{\text{FB}}$), the drain current is dominated by the ambipolar (hole-free carrier) leakage current from the drain to source ($I_{\text{D,leak}}$). Close to the flat band voltage, the subthreshold current ($I_{\text{sub-vt}}$) begins

to dominate, and above the threshold voltage, the drift current (I_{ON}) dominates.

1) On Current (I_{on}): The principal component of the above threshold dc current, I_{ON}, conveys the device performance in the linear (4) and saturation (5) regimes. The above-threshold currents are given by the following equations:

$$I_{ON} = \mu_{eff} C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2\alpha_{sat}}\right] \quad V_{DS} < \alpha_{sat}(V_{GS} - V_{th}) \tag{4}$$

$$I_{ON} = \frac{1}{2}\mu_{eff} C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2 \alpha_{sat} \quad V_{DS} \geq \alpha_{sat}(V_{GS} - V_{th}) \tag{5}$$

where C_{ox} is the oxide capacitance due to the top and bottom dielectric layers, V_{DS} is the drain bias, V_{GS} is the gate bias, V_{th} is the threshold voltage of the device, μ_{eff} is the effective charge carrier mobility, and α_{sat} is the saturation modulation parameter (the equations for which are described in the supplementary information). Table I shows the measured values of all the parameters used to describe (4) and (5). We discuss below the extraction of each of these parameters individually.

Fig. 2(f) and (i) shows the extracted V_{th} as a function of L for different W and as a function of V_{DS} for different L, exhibiting a negative shift for longer L, due to the filling of fewer oxygen vacancies and a positive shift for higher V_{DS} where oxygen vacancies are readily filled with electrons [40], [41], [42]. As the temperature increases, V_{th} initially decreased up to a transition temperature close to 45 °C, after which it began to increase. Therefore, accounting for all these effects, we can describe V_{th} as follows:

$$V_{th} = V_{th0} + \frac{1}{L}\left(A_t V_{DS}^2 + B_t\right) + \frac{C_t}{W} + K_{Vth}|t - 45| \tag{6}$$

where V_{th0} represents the threshold voltage of a very long channel device, where the impact of the S/D contacts on the channel is negligible. A_t and B_t model the dependence of V_{th} on V_{DS} and channel length, respectively, $K_{V_{th}}$ models the temperature dependence of the threshold voltage around the device transition temperature (45 °C) and C_t accounts for effects of W on V_{th} that originate from fringe fields at the edges of the channel that are more dominant at smaller W [43], [44], [45].

The TFT field-effect mobility can be modeled as a function of the channel length, the gate overdrive voltage ($V_{GS} - V_{th}$), and temperature. We observed an increase in the field-effect mobility with the channel length and substrate temperature, as shown in the bottom panels of Fig. 2(h) and (k). Therefore, accounting for these effects, we can determine an empirical equation for mobility as follows:

$$\mu_{eff} = [\mu_0 + k_3 L + k_4(T - 22)](V_{GS} - V_{th})^{\gamma} \tag{7}$$

where μ_0 is the field effect mobility for a hypothetical zero channel length device, k_3, and k_4 are the parameters modeling the dependence of the device mobility on the channel length and substrate temperature, and γ is the field effect mobility parameter.

The saturation modulation parameter models the dependence of the depletion charge density across the channel which can be modeled as follows:

$$\alpha_{sat} = \alpha_{sat0} + k_{\alpha sat} L + k_{\alpha T}(T - 22). \tag{8}$$

2) Subthreshold Current ($I_{sub\text{-}vt}$): The subthreshold current in the a-IGZO TFTs arises due to both the diffusion current generated by carriers in the interface trap states at the oxide–semiconductor interface and the drift current generated due to carriers in the bulk states in the channel [46]. The interface trap states at the Al_2O_3–a-IGZO boundary play an important role in the subthreshold current [47], [48]. Energy band-edge bending causes the interface states to be occupied first, and conduction occurs due to the thermal release of electrons from these states and to maintain overall charge neutrality in the device thereafter. The subthreshold diffusion current can be written as follows:

$$I_{sub\text{-}vt} = I_{OFF} \times \frac{W}{L} e^{\frac{q\phi_s}{kT}} \times \left(1 - e^{-\frac{qV_{DS}}{kT}}\right) \tag{9}$$

$$\phi_s = \frac{(V_{GS} - V_{FB})}{\left(1 + q^2 \frac{D_{it}}{C_{ox}}\right)} \tag{10}$$

where I_{OFF} is the drain current due to the intrinsic carrier density in the channel, kT/q is the thermal voltage and is equal to ~26 mV at room temperature, φ_s is the surface potential expressed, and D_{it} is the interface trap state density. The subthreshold ideality factor, η_i, is extracted from the subthreshold swing (SS) of the I–V curves [49], [50] using the following equation:

$$SS = \frac{kT}{q}\eta_i \ln(10) = 2.3\frac{kT}{q}\left(1 + q^2 \frac{D_{it}}{C_{ox}}\right). \tag{11}$$

SS is a function of the device dimensions as shown in Fig. 2(g). However, this method does not account for the change in the charged trap state density as a function of the gate bias and consequently, SS is assumed to be fixed over a wide V_{GS} range. Field-effect current measurements, high-frequency C–V measurements, and extractions based on device simulations have also been shown to be ineffective [51], [52], [53], [54], [55], [56]. Instead, we can calculate the flat band potential by simultaneously analyzing the measured I–V and C–V curves, as discussed in detail in the supplementary information [57], [58].

Once we accurately establish the flat band potential, we repeat the calculation for the surface potential as a function of the applied gate bias to extract the interface trap density below the threshold voltage using the following equation:

$$C_{ox}(V_{GS} - V_{FB} - \phi_s) = q\int_0^{q\phi_s} D_{it}(E)dE \approx q^2 D_{it}\phi_s \tag{12}$$

which assumes a uniformly distributed interface trap density in the energy bandgap. We extracted the dependence of D_{it} on $V_{GS} - V_{FB}$ for multiple channel lengths [Fig. 3(a)] and temperatures [Fig. 3(c)], and on φ_s [Fig. 3(b)]. To illustrate the effect of the variation of D_{it} on the simulated I–V curves, we compared the measured subthreshold current of a 100-/5-μm device against the simulated subthreshold current for a constant D_{it} extracted from the SS and for a voltage-dependent D_{it} extracted from the C–V curves. We observe a significantly better fit with a variable D_{it} especially as we

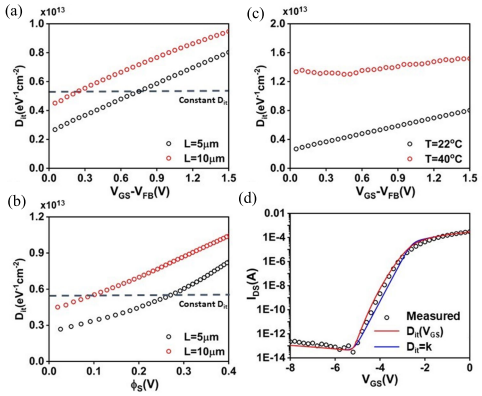

Fig. 3. Plot of the density of interface trap states (D_{it}) as a function of (a) $V_{GS} - V_{FB}$. (b) Surface potential φ_s, extracted from the C–V curves for a 100-/5-μm device. (c) Variation of the interface trap state density as a function of $V_{GS} - V_{FB}$ for two temperatures for a 100-/5-μm device. (d) Measured and simulated I–V curves for a 100-/5-μm device at $V_{DS} = 1$ V.

approach V_{th}, exhibiting a smooth transition from the interfacial trap state-dominated diffusion to bulk trap state-dominated drift current [Fig. 3(d)]. The drain and gate leakage currents are discussed in detail in the Acknowledgment and Table II.

C. Noise Characteristics (I_{noise})

Noise characterization is important for a TFT model, especially for applications involving the detection of signals in the μV and mV range. Our model accounts for both the flicker noise ($1/f$ noise), dominant at low frequencies and the white noise, dominant at frequencies above the corner frequency [59].

The white noise comprises shot noise due to the injection of carriers from the contacts into the channel and thermal noise of carriers in the channel. The shot noise is dominant at lower currents at V_{GS} near V_{th}, whereas the thermal noise is dominant at $V_{GS} \geq V_{th}$ where the channel conductivity increases. The white noise spectral density can be expressed as follows:

$$\frac{S_{iD}}{I_{DS}^2} = \frac{2q}{I_{DS}} + \frac{4kTg_{ch}\gamma_{white}}{I_{DS}^2} \tag{13}$$

where g_{ch} is the channel conductance, and γ_{white} is the thermal noise factor. The $1/f$ noise in the device is modeled using the original Hooge's equation for the device flicker noise [60], which is attributed to either carrier number fluctuation or bulk mobility fluctuation [61], [62], [63]. Noise in TFTs that operate with trap-based conduction through the interfacial defect states can be modeled by the carrier number fluctuation model [64], where the noise spectral density can be expressed as follows:

$$\frac{S_{iD}}{I_{DS}^2} = \frac{\alpha_H q}{C_{ox}WL(V_{GS} - V_{th})} \times \frac{1}{f} \tag{14}$$

where α_H is Hooge's parameter for noise. Table III shows the variation of the α_H with the device dimensions, temperature, and operation regimes. The noise power spectral density reduces with increasing device area, as shown in Fig. 4(a)–(d). We also observe a slight decrease in the normalized noise power spectral density with increasing temperature. These variations are modeled into (15) by extending the parametrization for Hooge's parameter. While α_H can vary with small process variations [60], we found that α_H variation with temperature is minimal in the linear regime and is significantly higher in the saturation regime and can be expressed as follows:

$$\alpha_{HS} = \alpha_{H0} + k_{\alpha H}(T - 22) \tag{15}$$

where α_{H0} is Hooge's parameter at room temperature, and $k_{\alpha H}$ accounts for the dependence of Hooge's parameter on temperature.

TABLE II
LEAKAGE PARAMETERS FOR THE DEVELOPED MODEL

Group	Parameter	Description	Value	Unit
Drain Leakage Current	I_{OL}	Drain Leakage Current Parameter for the	45	pA
	V_{DSL}	Variation of the Drain Leakage with Drain Bias	16.2	V
	V_{GSL}	Parameter for the Variation of the Drain Leakage with Gate Bias	24.75	V
Gate Leakage Current	$k_{gs,leak}$	Source Parameter for the Gate Leakage Current	2.091	aA/μm^2
	$k_{gd,leak}$	Drain Parameter for the Gate Leakage Current	-0.031	aA/μm^2
	V_{LGS}	Parameter for the Variation of the Gate Leakage with Gate-Source Bias	0.1869	V^{-1}
	V_{LGD}	Parameter for the Variation of the Gate Leakage with Gate-Drain Bias	0.6463	V^{-1}
Noise Current	α_{HL}	Linear Regime Hooge's Parameter	0.006	1
	α_{H0}	Room Temperature Saturation Regime Hooge's Parameter	0.0091	V^{-1}
	$k_{\alpha H}$	Parameter for the Variation of the Saturation Regime Hooge's Parameter	7.5×10^{-5}	°C

TABLE III
VARIATION OF HOOGE'S PARAMETER

W/L	Temperature	α_{HL} (Linear)	α_{HS} (Saturation)
100/5	RT	0.0061	0.0093
100/10	RT	0.0074	0.0102
100/15	RT	0.0045	0.0066
100/20	RT	0.006	0.0072
200/10	RT	0.0057	0.0091
500/10	RT	0.0048	0.0083
	40 °C	0.0058	0.0087
100/5	50 °C	0.0049	0.0077
	60 °C	0.0056	0.0063

D. Unity Gain Frequency (f_T)

We used conventional two-port scattering-parameter (s-parameter) measurements on the ground–signal–ground

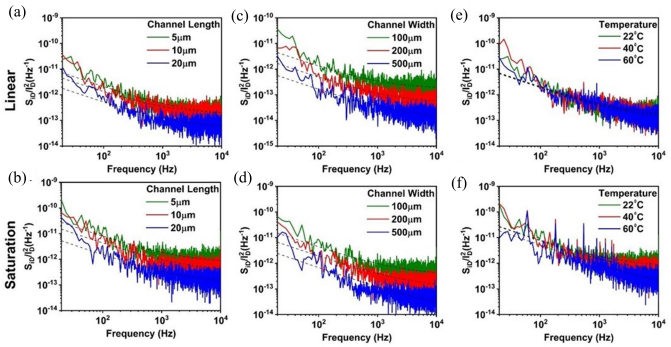

Fig. 4. Normalized spectral noise power density S_{ID} (A^2/Hz) with respect to the drain current (I_{DS}), plotted in the linear regime as a function of (a) channel length, (c) device width, and (e) temperature, and in the saturation regime as a function of (b) channel length, (d) device width, and (f) temperature. (e) and (f) Measured for a 100/5 μm device. The dotted lines show the fit noise spectra with our model.

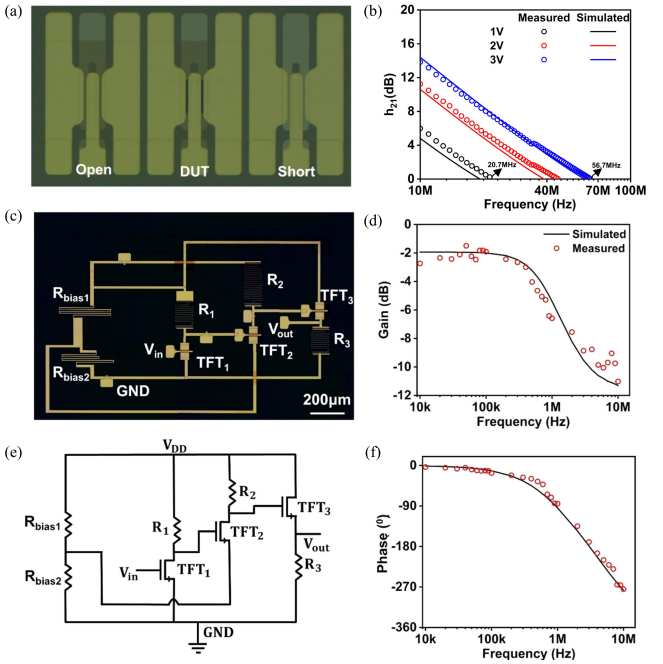

Fig. 5. (a) Optical microscope images of the GSG test patterns used to measure the unity gain frequency (f_T). (b) Plot of h_{21} versus frequency, measured and simulated, as a function of different V_{DS} and V_{GS}). (c) Optical microscope images of two-stage cascade amplifier circuit fabricated on polyimide and (d) its circuit schematics used for simulations. The measured values of the fabricated resistors were: R_{bias1} = 200 Ω, R_{bias2} = 500 Ω, R_1 = 22 kΩ, R_2 = 40 kΩ, and R_3 = 20 kΩ. (e) Plot of the amplitude of the gain as a function of frequency. (f) Plot of the phase as a function of frequency for the measured and simulated performance.

(GSG) test patterns to evaluate the f_T using well-established de-embedding procedures with control devices with no a-IGZO channel (open) and no gate dielectric (short), as shown in Fig. 5(a) [65]. We computed the forward current gain h-parameter, $h_{21} = i_D/i_G$, as shown in Fig. 5(b), and extrapolated h_{21} to 0 dB to extract f_T. f_T increases from 20.7 to 56.7 MHz as $V_{GS} = V_{DS}$ increased from 1 to 3 V consistent with an expected increase in the transconductance, g_m, with V_{DS}. Fig. 6(c) shows the small signal equivalent of

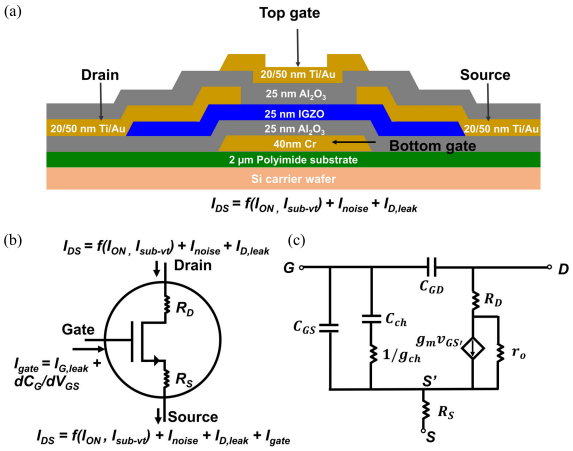

Fig. 6. (a) Schematic of the cross section of the dual gate a-IGZO TFT. (b) Overview of the equations used in the circuit modeling of the TFTs. (c) Small circuit model of the TFT, accounting for the effect of channel and gate capacitance and contact resistance on device performance.

the TFT model-accounting for the presence of the channel and gate capacitances (C_{GS} and C_{GD}) as well as the contact resistance (R_C).

III. Experimental Validation

A. Microfabrication Details

We fabricated dual gate TFTs on a 9-μm-thick polyimide film that was spun-cast and subsequently cured at 350 °C for 1 h in nitrogen ambient on a Si carrier wafer. Fig. 6(a) shows an illustrative schematic of the cross section of an a-IGZO TFT. We used atomic layer deposition (ALD) for 25-nm-thick aluminum oxide (Al_2O_3) dielectrics. We deposited 25-nm-thick a-IGZO thin films using radio frequency (RF) magnetron sputtering in an environment of 32.5% oxygen and 67.5% argon at 2 mtorr chamber pressure at 200 °C. The TFTs were characterized using an Agilent B1500A Semiconductor Parameter Analyzer for current voltage and capacitance–voltage measurements and with a National Instruments N9020A Spectrum Analyzer with an intermediate Stanford Research Systems SR570 Low Noise Current Preamplifier for noise characterization [66], [67]. s-parameters were measured using an Agilent E5071 Vector Network Analyzer, employing conventional GSG patterns. To account for variations in device parameters due to process variations, three devices with identical dimensions were characterized.

B. Circuit Verification

To validate the accuracy of our model, we fabricated a cascaded common-source amplifier with a common-drain voltage follower output buffer using a-IGZO TFTs and Ti thin film resistors that were encapsulated with ALD Al_2O_3 [Fig. 5(c)]. We then compared the amplifier's performance to computer simulations [Fig. 5(e)] that invoked our model. The simulation speed of our model is comparable to models of similar complexity, such as the EKV MOSFET model [28]. Our parametric model allows us to choose the most optimal

parameters for the circuit design, which is the added novelty introduced in this model. The circuit was designed to result in a gain of ∼1 V/V at the output to buffer the measured input signals. We measured the amplitude and phase of the input signal at V_{in} and the output signal at V_{out} as designated in Fig. 5(c). The magnitude of the gain $[20\log_{10}(V_{out}/V_{in})]$ in Fig. 5(d) and phase in Fig. 5(f) were in excellent agreement with simulations, demonstrating the comprehensiveness of our model in capturing the relevant large and small signal parameters for circuit design and operation.

IV. Conclusion

We report the development of a comprehensive physics-based a-IGZO TFT model that exploits empirical data measured across a wide range of device dimensions, multiple temperatures, and different operating regimes. The dual gate a-IGZO TFT test structures and circuits were fabricated on a flexible substrate, though we expect that the model will apply for a-IGZO TFTs fabricated on glass or other rigid substrates. The model incorporates all equations essential for reproducing the device performance in the subthreshold, linear, and saturation regimes. This model enables the a-IGZO TFT circuit level analysis for both dc and ac operation and enables a more thorough device and circuit design process. We predict that this model will pave the way for developing reliable circuits for normally-ON dual gate and single gate a-IGZO TFTs on flexible substrates for high-precision signal acquisition.

Acknowledgment

Supplemental information related to this publication is available on github upon request. The authors would like to thank the contribution of Dr. Hongseok Oh, to the process development training of Ritwik Vatsyayan on the fabrication of thin film transistors (TFTs). They would also like to thank the assistance of Po Chun Chen in the measurement of the cut-off frequency of the fabricated samples and discussions with Andrew Bourhis during the development of the model.

References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004.

[2] M. Mativenga, M. H. Choi, J. W. Choi, and J. Jang, "Transparent flexible circuits based on amorphous-indium–gallium–zinc–oxide thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 170–172, Feb. 2011, doi: 10.1109/LED.2010.2093504.

[3] H. Yabuta et al., "High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature RF-magnetron sputtering," *Appl. Phys. Lett.*, vol. 89, no. 11, pp. 10–13, Sep. 2006, doi: 10.1063/1.2353811.

[4] G. J. Lee, J. Kim, J.-H. Kim, S. M. Jeong, J. E. Jang, and J. Jeong, "High performance, transparent a-IGZO TFTs on a flexible thin glass substrate," *Semicond. Sci. Technol.*, vol. 29, no. 3, Mar. 2014, Art. no. 035003, doi: 10.1088/0268-1242/29/3/035003.

[5] M. M. Billah, M. M. Hasan, and J. Jang, "Effect of tensile and compressive bending stress on electrical performance of flexible a-IGZO TFTs," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 890–893, Jul. 2017, doi: 10.1109/LED.2017.2707279.

[6] D. H. Lee, K. Nomura, T. Kamiya, and H. Hosono, "Diffusion-limited a-IGZO/Pt Schottky junction fabricated at 200 °C on a flexible substrate," *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1695–1697, 2011, doi: 10.1109/LED.2011.2167123.

[7] J. Viventi et al., "Flexible, foldable, actively multiplexed, high-density electrode array for mapping brain activity in vivo," *Nature Neurosci.*, vol. 14, no. 12, pp. 1599–1605, Dec. 2011, doi: 10.1038/nn.2973.

[8] D. Bhatt, S. Kumar, and S. Panda, "Amorphous IGZO field effect transistor based flexible chemical and biosensors for label free detection," *Flexible Printed Electron.*, vol. 5, no. 1, Feb. 2020, Art. no. 014010, doi: 10.1088/2058-8585/ab724c.

[9] D. Geng, Y. F. Chen, M. Mativenga, and J. Jang, "Touch sensor array with integrated drivers and comparator using a-IGZO TFTs," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 391–394, Mar. 2017, doi: 10.1109/LED.2017.2661405.

[10] J. G. Troughton, P. Downs, R. Price, and D. Atkinson, "Densification of a-IGZO with low-temperature annealing for flexible electronics applications," *Appl. Phys. Lett.*, vol. 110, no. 1, pp. 1–10, Jan. 2017, doi: 10.1063/1.4973629.

[11] S. S. Chen and J. B. Kuo, "An analytical a-Si:H TFT DC/capacitance model using an effective temperature approach for deriving a switching time model," in *Proc. Int. Electron Devices Mater. Symp.*, Jul. 1994, p. 11, doi: 10.1109/EDMS.1994.863885.

[12] M. J. Izzard, P. M. P. Migliorato, and W. I. M. W. I. Milne, "A unified circuit model for the polysilicon thin film transistor," *Jpn. J. Appl. Phys.*, vol. 30, no. 2A, p. L170, Feb. 1991, doi: 10.1143/JJAP.30.L170.

[13] R. Martins et al., "Papertronics: Multigate paper transistor for multifunction applications," *Appl. Mater. Today*, vol. 12, pp. 402–414, Sep. 2018, doi: 10.1016/j.apmt.2018.07.002.

[14] E. Fortunato et al., "Zinc oxide, a multifunctional material: From material to device applications," *Appl. Phys. A, Solids Surf.*, vol. 96, no. 1, pp. 197–205, Jul. 2009, doi: 10.1007/s00339-009-5086-5.

[15] D. A. Mourey, D. A. Zhao, and T. N. Jackson, "Self-aligned-gate ZnO TFT circuits," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 326–328, Apr. 2010.

[16] H. Oh, G.-C. Yi, M. Yip, and S. A. Dayeh, "Scalable tactile sensor arrays on flexible substrates with high spatiotemporal resolution enabling slip and grip for closed-loop robotics," *Sci. Adv.*, vol. 6, no. 46, pp. 1–15, Nov. 2020.

[17] R. Brederlow et al., "Evaluation of the performance potential of organic TFT circuits," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, May 2003, pp. 378–500.

[18] A. Rahaman, Y. Chen, M. M. Hasan, and J. Jang, "A high performance operational amplifier using coplanar dual gate a-IGZO TFTs," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 655–661, 2019, doi: 10.1109/JEDS.2019.2923208.

[19] W. Chen et al., "Oxygen-dependent instability and annealing/passivation effects in amorphous In–Ga–Zn–O thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1552–1554, Nov. 2011, doi: 10.1109/LED.2011.2165694.

[20] E.-G. Chong, Y.-S. Chun, S.-H. Kim, and S.-Y. Lee, "Effect of oxygen on the threshold voltage of a-IGZO TFT," *J. Electr. Eng. Technol.*, vol. 6, no. 4, pp. 539–542, Jul. 2011, doi: 10.5370/JEET.2011.6.4.539.

[21] M. Estrada, A. Cerdeira, A. Ortiz-Conde, F. J. G. Sanchez, and B. Iñiguez, "Extraction method for polycrystalline TFT above and below threshold model parameters," *Solid State Electron*, vol. 46, no. 12, pp. 2295–2300, 2002, doi: 10.1016/S0038-1101(02)00186-7.

[22] L. Reséndiz, M. Estrada, and A. Cerdeira, "New procedure for the extraction of a-Si:H TFTs model parameters in the subthreshold region," *Solid State Electron*, vol. 47, no. 8, pp. 1351–1358, 2003, doi: 10.1016/S0038-1101(03)00070-4.

[23] G. W. Neudeck, K. Y. Chung, and H. F. Bare, "An accurate CAD model for the ambipolar a-Si:H TFT," *IEEE Trans. Electron Devices*, vol. ED-34, no. 4, pp. 866–871, Apr. 1987, doi: 10.1109/T-ED.1987.23008.

[24] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, "SPICE models for amorphous silicon and polysislicon thin film transistors," *J. Electrochem. Soc.*, vol. 144, no. 8, pp. 2833–2839, 1997.

[25] R. Shabanpour et al., "A transistor model for a-IGZO TFT circuit design built upon the RPI-aTFT model," in *Proc. 15th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2017, pp. 129–132, doi: 10.1109/NEWCAS.2017.8010122.

[26] C. Perumal et al., "A compact a-IGZO TFT model based on MOSFET SPICE level = 3 template for analog/RF circuit designs," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1391–1393, Nov. 2013, doi: 10.1109/LED.2013.2279940.

[27] T. Meister, K. Ishida, A. Sou, C. Carta, and F. Ellinger, "49.35 MHz GBW and 33.43 MHz GBW amplifiers in flexible a-IGZO TFT technology," *Electron. Lett.*, vol. 56, no. 15, pp. 782–785, Jul. 2020, doi: 10.1049/el.2020.0813.

[28] G. P. Patsis, "MOSFET EKV Verilog—A model implementation in Genesys," *IOSR J. VLSI Signal Process.*, vol. 8, no. 1, pp. 73–86, 2018.

[29] K.-H. Choi and H.-K. Kim, "Correlation between Ti source/drain contact and performance of InGaZnO-based thin film transistors," *Appl. Phys. Lett.*, vol. 102, no. 5, Feb. 2013, Art. no. 052103, doi: 10.1063/1.4790357.

[30] M. E. Rivas-Aguilar et al., "Specific contact resistance of IGZO thin film transistors with metallic and transparent conductive oxides electrodes and XPS study of the contact/semiconductor interfaces," *Current Appl. Phys.*, vol. 18, no. 7, pp. 834–842, Jul. 2018, doi: 10.1016/j.cap.2018.04.002.

[31] W.-S. Kim, Y.-K. Moon, K.-T. Kim, J.-H. Lee, B.-D. Ahn, and J.-W. Park, "An investigation of contact resistance between metal electrodes and amorphous gallium–indium–zinc oxide (a-GIZO) thin-film transistors," *Thin Solid Films*, vol. 518, no. 22, pp. 6357–6360, Sep. 2010, doi: 10.1016/j.tsf.2010.02.044.

[32] W. Wang et al., "Analysis of the contact resistance in amorphous InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 107, no. 6, pp. 1–15, Aug. 2015, doi: 10.1063/1.4928626.

[33] S. Luan and G. W. Neudeck, "An experimental study of the source/drain parasitic resistance effects in amorphous silicon thin film transistors," *J. Appl. Phys.*, vol. 72, no. 2, pp. 766–772, Jul. 1992, doi: 10.1063/1.351809.

[34] H. Klauk et al., "Contact resistance in organic thin film transistors," *Solid-State Electron.*, vol. 47, pp. 297–301, Feb. 2003, doi: 10.1016/S0038-1101(02)00210-1.

[35] G. K. Reeves and H. B. Harrison, "Obtaining the specific contact resistance from transmission line model measurements," *IEEE Electron Device Lett.*, vol. EDL-3, no. 5, pp. 111–113, May 1982, doi: 10.1109/EDL.1982.25502.

[36] H. H. Berger, "Contact resistance and contact resistivity," *J. Electrochem. Soc.*, vol. 119, no. 4, p. 507, 1972, doi: 10.1149/1.2404240.

[37] J. S. Lee, S. Chang, H. Bouzid, S.-M. Koo, and S. Y. Lee, "Systematic investigation on the effect of contact resistance on the performance of a-IGZO thin-film transistors with various geometries of electrodes," *Phys. Status Solidi, A*, vol. 207, no. 7, pp. 1694–1697, Jul. 2010, doi: 10.1002/pssa.200983753.

[38] Q. Guo, F. Lu, Q. Tan, T. Zhou, J. Xiong, and W. Zhang, "Al_2O_3-based a-IGZO Schottky diodes for temperature sensing," *Sensors*, vol. 19, no. 2, p. 224, Jan. 2019, doi: 10.3390/s19020224.

[39] D. Esseni and F. Driussi, "A quantitative error analysis of the mobility extraction according to the Matthiessen rule in advanced MOS transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2415–2422, Aug. 2011, doi: 10.1109/TED.2011.2151863.

[40] D. H. Kang, J. U. Han, M. Mativenga, S. H. Ha, and J. Jang, "Threshold voltage dependence on channel length in amorphous-indium–gallium–zinc–oxide thin-film transistors," *Appl. Phys. Lett.*, vol. 102, no. 8, Feb. 2013, doi: 10.1063/1.4793996.

[41] S. H. Ha, D. H. Kang, I. Kang, J. U. Han, M. Mativenga, and J. Jang, "Channel length dependent bias-stability of self-aligned coplanar a-IGZO TFTs," *J. Display Technol.*, vol. 9, no. 12, pp. 985–988, Dec. 2013.

[42] Y. Nam, H.-O. Kim, S. H. Cho, and S.-H. K. Park, "Effect of hydrogen diffusion in an In–Ga–Zn–O thin film transistor with an aluminum oxide gate insulator on its electrical properties," *RSC Adv.*, vol. 8, no. 10, pp. 5622–5628, 2018, doi: 10.1039/c7ra12841j.

[43] G. Wu, A. Sahoo, D. Chen, and J. Chang, "A comparative study of E-beam deposited gate dielectrics on channel width-dependent performance and reliability of a-IGZO thin-film transistors," *Materials*, vol. 11, no. 12, p. 2502, Dec. 2018, doi: 10.3390/ma11122502.

[44] K.-H. Liu et al., "Investigation of channel width-dependent threshold voltage variation in a-InGaZnO thin-film transistors," *Appl. Phys. Lett.*, vol. 104, no. 13, pp. 1–5, Mar. 2014, doi: 10.1063/1.4868430.

[45] S. H. Choi and M. K. Han, "Effect of channel widths on negative shift of threshold voltage, including stress-induced hump phenomenon in InGaZnO thin-film transistors under high-gate and drain bias stress," *Appl. Phys. Lett.*, vol. 100, no. 4, pp. 10–13, 2012, doi: 10.1063/1.3679109.

[46] S. Lee, S. Jeon, and A. Nathan, "Modeling sub-threshold current–voltage characteristics in thin film transistors," *J. Display Technol.*, vol. 9, no. 11, pp. 883–889, Nov. 2013, doi: 10.1109/JDT.2013.2256878.

[47] H.-H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, and C.-C. Wu, "Modeling of amorphous $InGaZnO_4$ thin film transistors and their subgap density of states," *Appl. Phys. Lett.*, vol. 92, no. 13, pp. 10–13, Mar. 2008, doi: 10.1063/1.2857463.

[48] S. H. Chen, S. C. Ho, C. H. Chang, C. C. Chen, and W. C. Say, "Influence of roughness on in-vivo properties of titanium implant surface and their electrochemical behavior," *Surf. Coat. Technol.*, vol. 302, pp. 215–226, Sep. 2016, doi: 10.1016/j.surfcoat.2016.06.007.

[49] S. H. Rha et al., "Performance variation according to device structure and the source/drain metal electrode of a-IGZO TFTs," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3357–3363, Dec. 2012, doi: 10.1109/TED.2012.2220367.

[50] S. Lee, "Bias-dependent subthreshold characteristics and interface states in disordered semiconductor thin-film transistors," *Semicond. Sci. Technol.*, vol. 34, no. 11, Nov. 2019, Art. no. 11LT01, doi: 10.1088/1361-6641/ab4298.

[51] M. Shur and M. Hack, "Physics of amorphous silicon based alloy field-effect transistors," *J. Appl. Phys.*, vol. 55, no. 10, pp. 3831–3842, May 1984, doi: 10.1063/1.332893.

[52] L. M. Terman, "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes," *Solid-State Electron.*, vol. 5, no. 5, pp. 285–299, Sep./Oct. 1962, doi: 10.1016/0038-1101(62)90111-9.

[53] T. K. A. Chou and J. Kanicki, "Two-dimensional numerical simulation of solid-phase-crystallized polysilicon thin-film transistor characteristics," *Jpn. J. Appl. Phys.*, vol. 38, no. 4, pp. 2251–2255, 1999, doi: 10.1143/jjap.38.2251.

[54] M. J. Powell, "The physics of amorphous-silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 12, pp. 2753–2763, Dec. 1989.

[55] D.-H. Kim et al., "Dissolvable films of silk fibroin for ultrathin conformal bio-integrated electronics," *Nature Mater.*, vol. 9, no. 6, pp. 511–517, Jun. 2010, doi: 10.1038/nmat2745.

[56] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono, "Trap densities in amorphous-$InGaZnO_4$ thin-film transistors," *Appl. Phys. Lett.*, vol. 92, no. 13, pp. 1–4, Mar. 2008, doi: 10.1063/1.2904704.

[57] P. Migliorato, M. Seok, and J. Jang, "Determination of flat band voltage in thin film transistors: The case of amorphous-indium gallium zinc oxide," *Appl. Phys. Lett.*, vol. 100, no. 7, pp. 1–10, Feb. 2012, doi: 10.1063/1.3685705.

[58] H. Oh and S. A. Dayeh, "An analytical model for dual gate piezoelectrically sensitive ZnO thin film transistors," *Adv. Mater. Technol.*, vol. 6, no. 8, Aug. 2021, Art. no. 2100224, doi: 10.1002/admt.202100224.

[59] R. Sarpeshkar, T. Delbruck, and C. A. Mead, "White noise in MOS transistors and resistors," *IEEE Circuits Devices Mag.*, vol. 9, no. 6, pp. 23–29, Nov. 1993, doi: 10.1109/101.261888.

[60] F. N. Hooge, "1/f noise sources," *Proc. IEEE*, vol. 70, no. 3, pp. 1926–1935, Nov. 1982.

[61] A. Corradetti et al., "Evidence of carrier number fluctuation as origin of 1/f noise in polycrystalline silicon thin film transistors," *Appl. Phys. Lett.*, vol. 67, no. 12, pp. 1730–1732, Sep. 1995, doi: 10.1063/1.115031.

[62] A. A. Balandin, "Low-frequency 1/f noise in graphene devices," *Nature Nanotechnol.*, vol. 8, no. 8, pp. 549–555, Aug. 2013, doi: 10.1038/nnano.2013.144.

[63] E. P. Vandamme and L. K. J. Vandamme, "Critical discussion on unified 1/f noise models for MOSFETs," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2146–2152, 2000, doi: 10.1109/16.877177.

[64] L. K. J. Vandamme, X. Li, and D. Rigaud, "1/f noise in MOS devices, mobility or number fluctuations?" *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1936–1945, Nov. 1994, doi: 10.1109/16.333809.

[65] E. P. Vandamme, D. M. M.-P. Schreurs, and G. Van Dinther, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 737–742, Apr. 2001, doi: 10.1109/16.915712.

[66] C. G. Theodorou et al., "Origin of low-frequency noise in the low drain current range of bottom-gate amorphous IGZO thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 898–900, Jul. 2011, doi: 10.1109/LED.2011.2143386.

[67] J. C. Park et al., "Low-frequency noise in amorphous indium–gallium–zinc oxide thin-film transistors from subthreshold to saturation," *Appl. Phys. Lett.*, vol. 97, no. 12, pp. 2008–2011, 2010, doi: 10.1063/1.3491553.