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A 0.00179 mm^2/Ch Chopper-Stabilized TDMA Neural Recording System with Dynamic EOV Cancellation and Predictive Mixed-Signal Impedance Boosting

Nader Sherif Kassem Fathy, Ritwik Vatsyayan, Andrew M. Bourhis, *Graduate Student Members, IEEE*, Shadi A. Dayeh, and Patrick P. Mercier, *Senior Member, IEEE*

***Abstract*— This article presents a digitally-assisted multi-channel neural recording system. The system uses a 16-channel chopper-stabilized Time Division Multiple Access (TDMA) scheme to record multiplexed neural signals into a single shared analog front end (AFE). The choppers reduce the total integrated noise across the modulated spectrum by 2.4× and 4.3× in Local Field Potential (LFP) and Action Potential (AP) bands, respectively. In addition, a novel impedance booster based on Sign-Sign least mean squares (LMS) adaptive filter (AF) predicts the input signal and pre-charges the AC-coupling capacitors. The impedance booster module increases the AFE input impedance by a factor of 39× with a 7.1% increase in area. The proposed system obviates the need for on-chip digital demodulation, filtering, and remodulation normally required to extract Electrode Offset Voltages (EOV) from multiplexed neural signals, thereby achieving 3.6× and 2.8× savings in both area and power, respectively, in the EOV filter module. The Sign-Sign LMS AF is reused to determine the system loop gain, which relaxes the feedback DAC accuracy requirements and saves 10.1× in power compared to conventional oversampled DAC truncation-error ΔΣ-modulator. The proposed SoC is designed and fabricated in 65 nm CMOS, and each channel occupies 0.00179 mm^2 of active area. Each channel consumes 5.11 μW of power while achieving 2.19 μV_{rms} and 2.4 μV_{rms} of input referred noise (IRN) over AP and LFP bands. The resulting AP band noise efficiency factor (NEF) is 1.8. The proposed system is verified with acute *in-vivo* recordings in a Sprague-Dawley rat using parylene C based thin-film platinum nanorod microelectrodes.**

***Index Terms*—Multi-Channel neural recording system, impedance boosting, implantable Brain-Machine Interface (BMI), electrocorticography (ECoG), time-division multiple access (TDMA), digitally assisted Sign-Sign least mean square (LMS) adaptive filter (AF).**

I. Introduction

THE simultaneous recording of many neural channels in parallel has recently emerged as an active area of research in neuroscience. High-density neural interfaces encounter spatial constraints due to the active area of each recording channel analog front-end (AFE). Recent advances in materials and integration technologies have enabled the development of high-density, high channel count neural interfaces [1]. Despite the progress in on-device electronics as well as the development of high-density flex to rigid bonding interfaces [2], [3], [4], the large active area of the AFE remains a critical bottleneck.

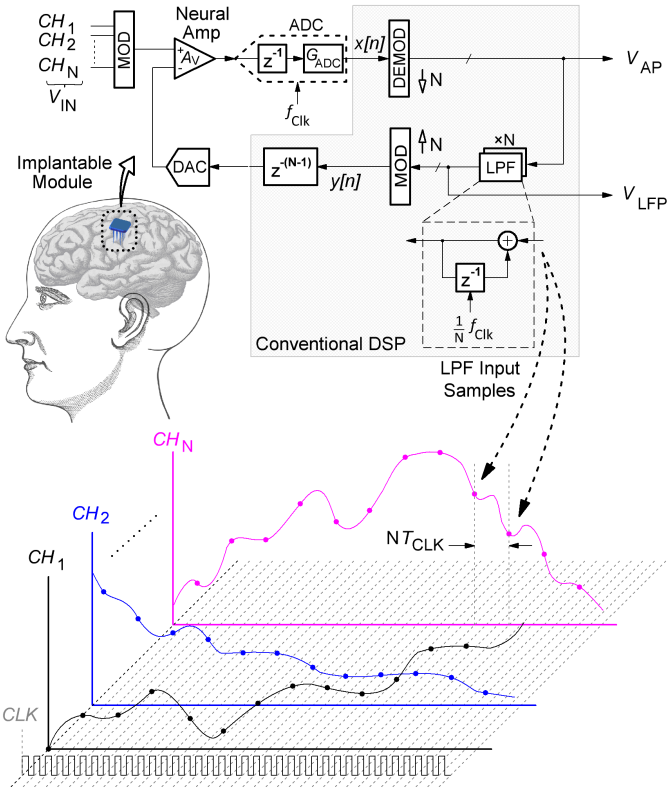

Fig. 1 Conventional multiple access mechanism neural recording system block diagram.

Researchers studying the vertebrate brain are required to analyze data from massively high-density cortical cells such as those in the visual (V1) and motor (M1) cortex, and there exists a need to improve the spatial resolution of recording channels [5], [6], [7], [8]. Enhancing our understanding of the human nervous system can pave the way for the development of treatment paradigms for disorders such as blindness, epilepsy, multiple sclerosis, Parkinson's, and potentially Alzheimer's Disease [9], [10], [11]. According to a 2021 study, in the United States alone, there are more than 53 million people living with these neurological conditions, which cost the economy more than $1.5 trillion annually [12]. Technological advancements that can serve to prevent and treat this impacted population hold the potential of increasing the wellness of subjects and their

caregivers in addition to reducing the economic burden. High performance recording systems with high spatial resolution are at the heart of these needed advances. To achieve higher spatial resolution in neural recording, a high-channel-count neural acquisition AFE module is imperative within a confined spatial area, while also necessitating support for high temporal resolution for µECoG neural acquisition. This includes coverage of both local field potential (LFP) (1 – 300 Hz) and action potential (AP) (300 Hz – 10 kHz) bands with amplitudes in the range of 10 μV- 1 mV [13], [14].

One potential solution to design area-efficient and low-power neural recording systems is through a multiple-access modulation scheme, where the entire AFE is shared between *N*-channels [15], [16], [17], [18]. However, several challenges persist. 1) The dynamic electrochemical reactions at the interface of the neural electrodes and tissue lead to a slowly varying electrode offset voltage (EOV) between electrodes that can reach magnitudes as high as ±50 mV [13], [14], [19], [20]. When these voltages are directly coupled onto the multiplexer, they can easily saturate the AFE and cause loss of neural recording functionality. As a result, area-consuming low-pass filters (LPFs), digital multiplexer (MUX), demultiplexer (DEMUX), and least mean square (LMS) adaptive filter (AFs) that extract, process, and feed back EOV data to the AFE are needed. It should be noted that traditional AC-coupled AFEs, DC-servo loops, and filtering techniques, which have been previously established in the literature to extract the neural signal from the undesired EOV artifact [13], [20], [21] are mostly effective in in-pixel architectures, where each channel is recorded by an individual AFE, and thus are not applicable here. 2) Multiplexing *N* electrodes requires an amplifier bandwidth (BW) at least *N* times larger, which forces the amplifier's input differential-pair to be small to achieve the larger BW at low currents, and therefore increases the worst-case 1/*f* noise corner frequency, especially in scaled CMOS technologies (e.g., 290 kHz in the proposed design in 65 nm CMOS). 3) Multiplexing spreads 90% of the signal energy of all channels from ~DC to ~860 kHz for *N*=16, and thus makes 1/*f* noise a larger component of the total noise, especially for AP recording up to 10 kHz [22]. 4) Chopping after a MUX to reduce the impact of 1/*f* noise degrades input impedance more than just multiplexing. As a result of these challenges, most time-division multiple-access (TDMA) neural recording systems either limit their BW to 500 Hz [18], occupy a larger than necessary area, or present more noise efficiency factor (NEF) than desired.

Fig. 1 shows a conventional digital signal processing (DSP) in a multiple-access scheme biosensor system, where the input channels are up-modulated in the analog domain such that they can all be amplified and digitized by a single shared amplifier and analog to digital converter (ADC). ADC samples are then sent to a DSP module to down-convert each channel's samples to baseband. At this point, the DSP can perform some signal processing to isolate the slowly-varying EOV from the neural signals, typically via a *N*-multiple of LPFs implemented as integrators. This information can then be fed back to the neural amplifier front-end to subtract the EOV on a per-channel basis via a high-resolution digital to analog converter (DAC) [15], [18]. However, per-channel subtraction requires up-modulation of each of the EOV cancellation signals in order to match the effective sampling frequency of the input signals at the amplifier input (i.e., after the input multiplexer). Accordingly, an N-1 delay block is added to the feedback path. The extraction of EOV poses challenges due to the requirement of on-chip demodulators, digital LPFs, and modulators, leading to high digital power consumption and increased area for each channel.

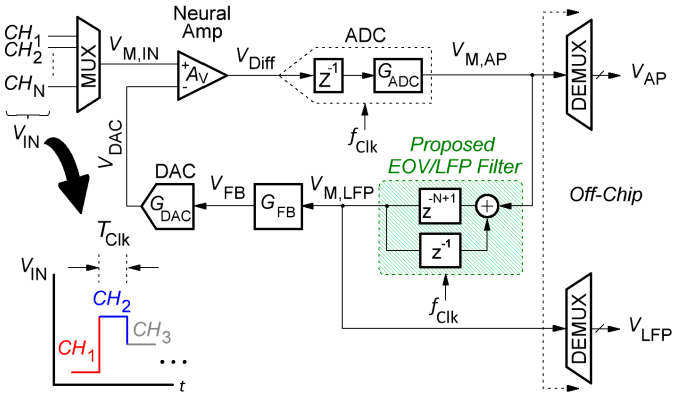

Fig. 2 Proposed neural recording system block diagram with direct EOV/LFP filter.

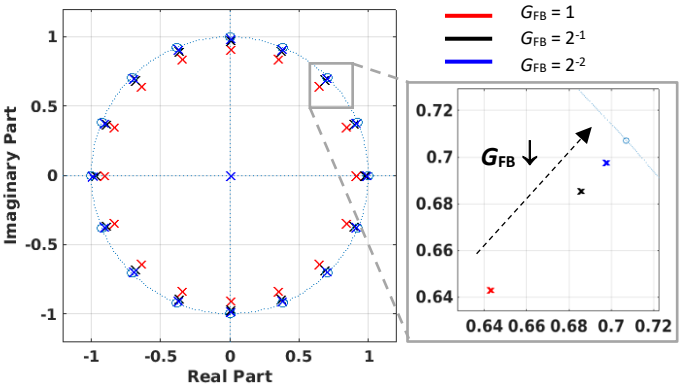

Fig. 3 Proposed system Z-Plane poles and zeros for stability analysis with various values of $G_{FB} = \{1, 2^{-1}, 2^{-2}\}$.

With high neural amplifier mid-band gain factors that usually exceeds 40 dB on typical small voltage supplies of 1.2 V, the amplifier can saturate on signals of >5 mV_p. Additionally, the AFE input referred noise (IRN) is usually required to be less than 5 μV_{rms}. Together, these two specifications require a high DAC resolution of at least 18 bits in feedback to suppress quantization noise, caused by EOV removal, below the thermal noise floor. Prior-art systems [13] use coarse and fine DACs in feedback in addition to ΔΣ-modulators to increase the effective number of bits (ENOB) of a small-area DAC [15], [23]. Unfortunately, these approaches result in a high per-channel power and area consumption [18].

To address these challenges, this paper introduces a TDMA-based neural recording mixed-signal front-end that: 1) utilizes a direct EOV/LFP filter that extracts and eliminates the EOV/LFP from modulated neural signals while operating at the same clock rate as the ADC without requiring on-chip modulation, demodulation, and individual LPFs, reducing the

number of adders by 15× and cumulatively saving 3.6× and 2.8× in the area and power of the EOV/LFP filter module, respectively, when compared to the solution in [15]; 2) splits the MSBs and LSBs of the EOV/LFP feedback DAC into the digital and analog domains that, when combined with a digital Sign-Sign LMS filter with a dither calibration signal running at the ADC clock rate, relaxes the DAC requirements and saves 10.1× in power compared to the conventional oversampled DAC truncation-error DS-modulator [15]; 3) adds chopper stabilization after the MUX to reduce the total integrated noise across the modulated spectrum by 2.4× and 4.3× in LFP and AP bands, respectively; 4) reuses the sign-sign LMS AF to predict the input signal, whose output is then used to pre-charge the input AC capacitors via the existing mixed-signal feedback architecture and improve the input impedance by 39×, all with only a 7.1% increase in area.

The paper is organized as follows: In Section II, a study of the proposed neural recording system is presented. In Section III, the design architecture is introduced. In Section IV, the circuit implementations are illustrated. Finally, the measurement results and conclusion are discussed in Section V and VI, respectively.

II. Proposed Neural Recording System Modules

Conventional multiple-access schemes used in neural recording systems, as depicted in Fig. 1, suffer from several issues. These issues encompass the use of redundant LPFs across *N*-channels, a considerable feedback DAC size, and the presence of flicker noise in the wide bandwidth neural amplifier. It is crucial to take these factors into account when designing neural recording systems to minimize the IRN and achieve the desired signal quality.

A. EOV/LFP Feedback Filter

The DSP block depicted in Fig. 1 features redundant LPFs, which is known to consume a considerable amount of digital power and area. For example, when implemented in 65 nm CMOS technology for N=16 channels, the EOV/LFP digital module occupies an area of ~0.016 mm^2 and the power consumption in ~19 µW [15]. This work proposes a novel solution in the form of a direct EOV/LFP digital filter, which offers equivalent functionality to the aforementioned DSP block while minimizing power and area overhead.

To explain the redundancy in the conventional systems shown in Fig. 1, consider the path of the neural signals from the ADC to the feedback DAC. After the ADC samples all *N* input channels in a time-multiplexed manner, the demodulator lowers the sampling rate of each channel by a factor of *N*; this forces the LPFs (integrators) to stay idle for $N \times T_{CLK}$, where f_{CLK} is the ADC clock frequency. To avoid signal aliasing, the ADC sampling rate is set to $f_{CLK} = 2\,N\,f_{BW}$, where f_{BW} is the neural signal BW. The extracted EOV from the LPFs are then up-modulated and fed to a DAC to be subtracted from the neural amplifier.

In contrast, Fig. 2 shows the proposed neural recording system with a direct EOV/LFP digital filter. The proposed filter operates at the same clock frequency as the ADC and extracts

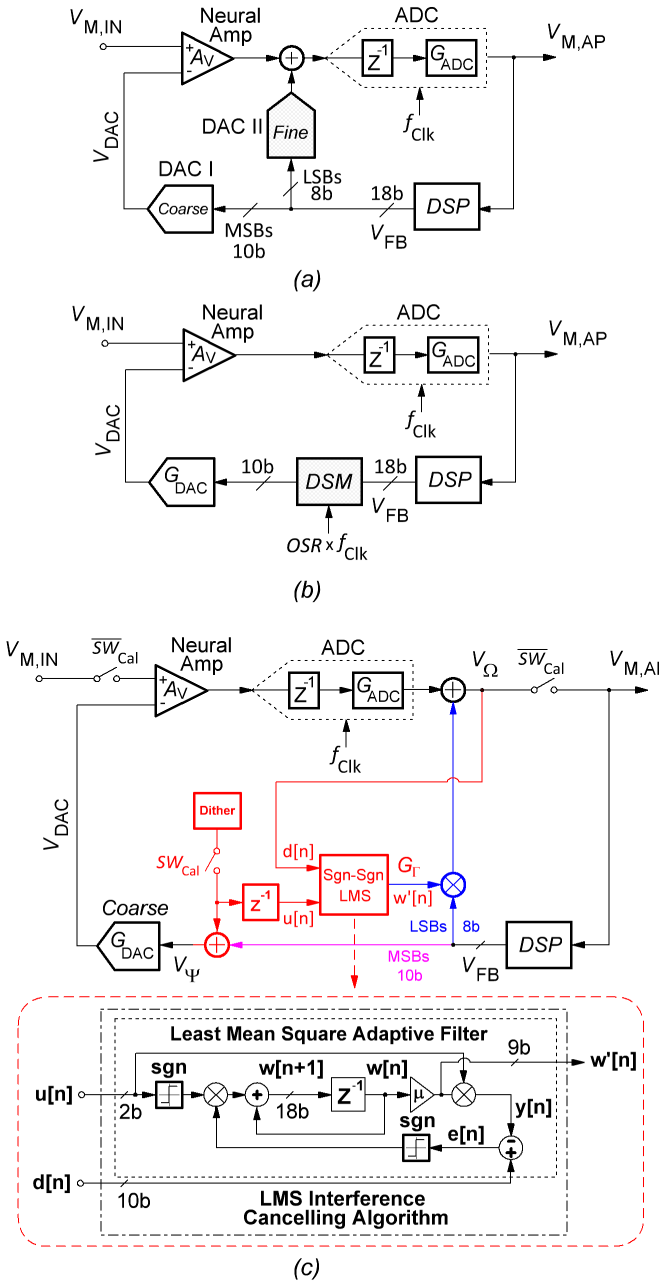

Fig. 4 Block diagram representation of feedback DAC in prior-art (a) using coarse and fine DACs [13], [16]; (b) using a ΔΣ truncation error DAC; and (c) proposed DAC size reduction system block diagram via Sign-Sign LMS AF.

the EOV/LFP directly, and thus the functionality of the proposed filter is similar to the DSP module on the path from x[n] to y[n] shown in Fig. 1. Since the ADC introduces 1-unit T_{CLK} delay of 3.125 µs, the proposed filter adds (*N*-1)-unit delays such that the overall EOV/LFP loop undergoes *N*-unit delay. This delay is necessary because the EOV/LFP feedback loop output-samples must align with the input multiplexed samples of EOV/LFP. The proposed EOV/LFP filter in Fig. 2 occupies an active area of 0.00425 mm^2 and consumes 6.8 µW for N=16 channels. The proposed digital filter hence removes the redundant LFPs and saves N-1 digital full-adders when

compared to conventional systems [15]. Furthermore, it offers the advantage of eliminating the need for EOV-modulators and demodulators. The total area and power savings in the EOV/LFP module is 3.68× and 2.8×, respectively.

To study the stability of the system with the proposed EOV/LFP filter, assume a linear system with block gains of A_v, G_{ADC}, G_{FB}, and G_{DAC} for the neural amplifier, the ADC, the feedback bandwidth controller, and the DAC, respectively. G_{FB} is added to provide an extra degree of freedom to easily control the bandwidth while maintaining system stability. By applying Mason's gain formula, the overall system block diagram transfer function is derived as,

$$H(z) = \frac{V_{M,AP}}{V_{M,IN}} = \frac{A_v\, G_{ADC}\, z^{-1}\,(1 - z^{-N})}{1 + (A_v\, G_{ADC}\, G_{FB}\, G_{DAC} - 1)\, z^{-N}}$$

$$= \frac{\sigma\, z^{-1}\,(1 - z^{-N})}{1 + \zeta\, z^{-N}} \quad (1)$$

where $\sigma = A_v\, G_{ADC}$, and $\zeta = A_v\, G_{ADC}\, G_{FB}\, G_{DAC}$ - 1. Fig. 3 shows the proposed system's poles and zeroes, for $N = 16$ channels, $A_v = 200$, $G_{ADC} = 2^{10}$, and $G_{DAC} = 2^{-18}$. Then, the system stability can be analyzed with various feedback gain values for $G_{FB} = \{1, 2^{-1}, 2^{-2}\}$. The system remains stable if the term $|\zeta| \leq 1$, since the parameters A_v, G_{ADC}, and G_{DAC} have their values set to achieve specific system performances. The parameter ζ also controls the high-pass cutoff frequency of the action potential (AP) band, as seen in Fig. 3. As the poles approaches the unit circle by decreasing G_{FB}, the high-pass cutoff is pushed to lower frequencies. The parameter G_{FB} is set such that the LFP band is set to ~300 Hz. It is imperative that the stability requirement of $|\zeta| \leq 1$ is satisfied across corners during system design. Otherwise, an adaptive filter (AF) will be required to guarantee stability with the highest loop gain [15].

B. Feedback DAC Resolution

Neural recording systems usually operate on low supply voltages of less than 1.2 V and require an IRN less than 5 μV_{rms}, [15], [18], [13], [23]. The feedback DAC injects its output directly at the input of the AFE, hence sets strict requirements for the quantization noise produced during digital and analog subtraction of EOV/LFP signals from the AFE input. To fulfill the noise criterion mentioned earlier in Section I, the feedback DAC should have a precision of at least 18 bits. Fig. 4(a) shows a conventional solution to relax the DAC requirements by using a coarse and fine DAC in feedback. The fine DAC is relaxed as it benefits from the gain of the neural amplifier. However, two problems arise from this architecture: 1) more active area is required to implement both DACs; 2) the fine DAC LSBs must be multiplied by a digital gain of -1 × $G_{DAC\text{-}I}$ × A_V to get the accuracy required, however, the coarse DAC and neural amplifier gains are affected by process mismatch which will introduce non-linearity to the recorded neural signal [16], [13]. Fig. 4(b) shows prior-art solution where a truncation error ΔΣ modulator is used, the ΔΣ is operating with an oversampling ratio (OSR) of higher than 32 × f_{CLK} [15]. The later reduces the active area, but it requires higher power consumption due to the digital dynamic power dissipation C×V^2×(32f_{CLK}).

Fig. 4(c) shows the proposed solution that eliminates the use of fine/coarse DACs or ΔΣ-modulators, which ultimately relaxes the DAC requirements from 18-bits to 10-bits. Since the DSP output signal, $V_{FB,}$ is 18-bits, the signal can be split into a coarse 10-bits MSBs and fine 8-bits LSBs. If the gain path defined as $G_\Gamma = V_\Omega / V_\Psi$ is determined, then the LSBs can be subtracted in the digital domain instead of the analog domain, whereas the MSBs are set to be large enough to drive the neural amplifier out of saturation caused by EOV signals. To determine G_Γ on system startup, a calibration mode initiates with SW_{Cal} set to logic high. A digital ±1 dither signal is injected through the coarse DAC, and a delayed version of the dither is injected to *u[n]* port of a Sign-Sign LMS AF. The AF is connected in an interference-cancelling scheme. The injected dither is recorded by the ADC and fed into the *d[n]* port of the AF. The AF then compares the original dither to the amplified dither and determines the gain factor by the interference-canceling algorithm following:

$$w[n+1] = w[n] + \; Sgn(u[n])\, Sgn(d[n] - y[n]) \quad (2)$$

where the *Sgn* operator is defined as

$$Sgn(x) = \begin{cases} 1; & x > 0 \\ 0; & x = 0 \\ -1; & x < 0 \end{cases}$$

The gain block μ is a constant set by the designer which controls speed and accuracy of the AF. Once the AF converges, SW_{Cal} switches to logic low and the AF *w'[n]* port exports the path gain defined as

$$G_\Gamma = G_{DAC}\, A_v\, G_{ADC} \quad (3)$$

Afterwards, G_Γ is sampled and stored, then the calibration module is powered down to save power. V_{FB} LSBs are multiplied by G_Γ and added to the ADC output. The Sign-Sign LMS is considered one of the simplest AF as it consists of two sign-multipliers; *u[n]* is ±1 dither signal and is connected to both multipliers. The factor μ is implemented as a right-shift operator by 9-bits.

On comparing a digitally synthesized ΔΣ modulator operating at 32 × f_{Clk} with the proposed Sgn-Sgn LMS running at f_{Clk}, the overall digital module area of the proposed technique is observed to be higher by a factor of 3×. Nonetheless, the power consumption is significantly reduced by a factor of 10.1×. The proposed approach is regarded as superior due to its utilization of an f_{Clk} of 320 kHz, whereas the ΔΣ modulator necessitates an on-chip clock generator functioning at 10.24 MHz. Additionally, the parameter G_{FB} is automatically set since the loop gain G_Γ is determined after calibration without the need for full LMS AF as proposed in [15].

C. Neural Amplifier Flicker Noise

In multiple-access neural recording AFEs, the neural amplifier

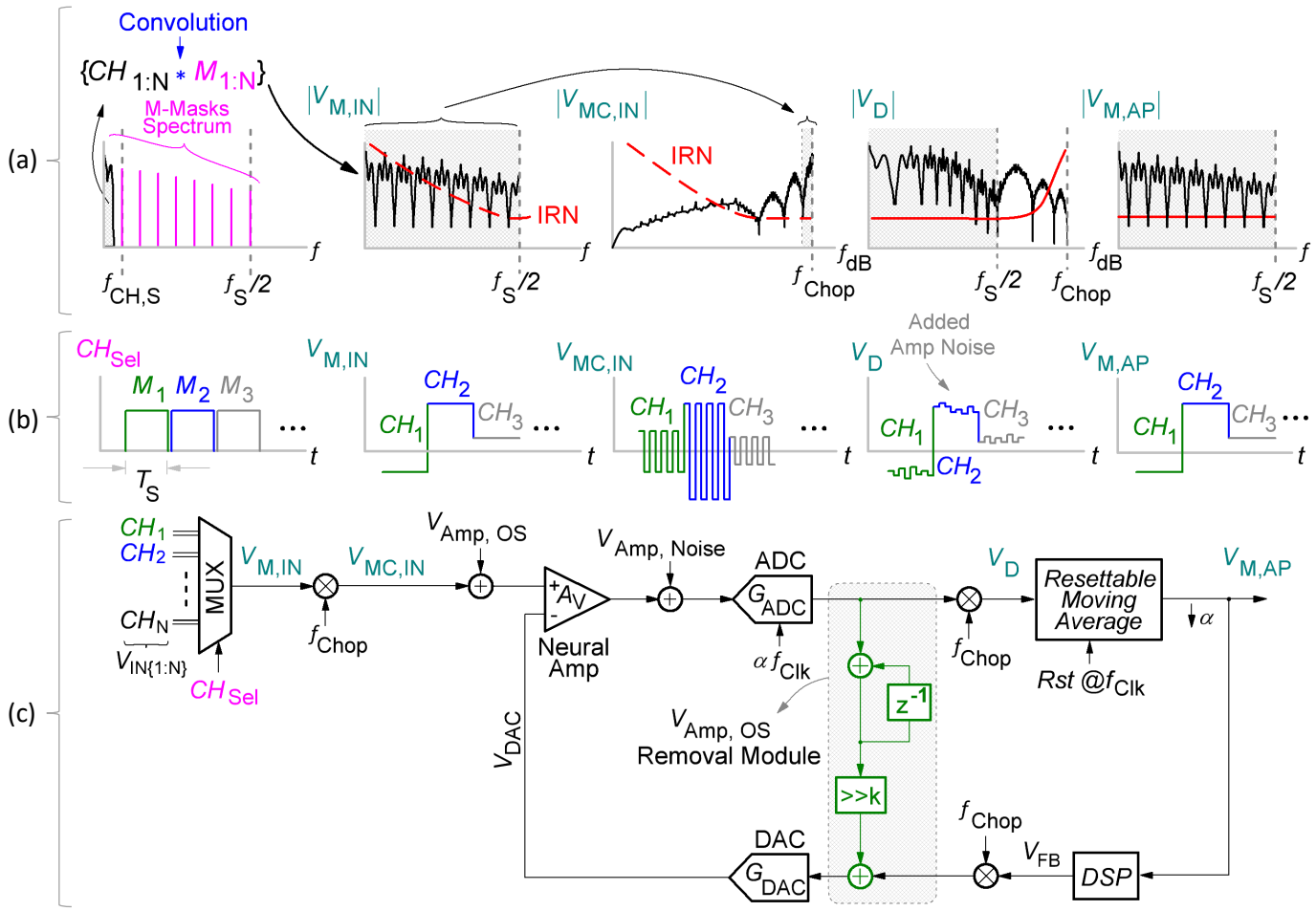

Fig. 5 Proposed chopping solution for TDMA neural recording system showing (a) the signal frequency domain representation across various points in the system, (b) the signal time domain representation, and (c) the system block diagram.

open-loop 3-dB BW must pass the up-modulated analog signal without introducing distortion or noise exceeding a few microvolts [13]. These requirements create a tradeoff between the required input diff-pair size; the smaller the device sizes the higher achieved BW, but also the higher the 1/*f* noise corner frequency. In TDMA systems, time multiplexing spreads signal content of all channels from DC to ~860 kHz, which is 90% of the energy bandwidth of the signal spectrum for *N*=16 channels. This makes the worst-corner amplifier 1/*f* noise corner frequency increase: for example, up to 290 kHz in this work, which is ~33% of the modulated signal bandwidth of ~860 kHz. To break this tradeoff, the 1/*f* noise can be attenuated by using chopper-stabilization, which up-modulates the already-multiplexed neural signals to a band higher than the flicker corner frequency.

In this work, the proposed system utilizes a chopper placed after the analog multiplexer. Fig. 5 demonstrates the chopper-stabilized neural recording system block diagram, showing how the (already multiplexed) input signal that is multiplexed at frequency f_S = 320 kHz is up modulated by an analog chopper with non-overlapping clock generated by the on-chip DSP module of frequency f_{Chop} = 1.28 MHz. This translates the

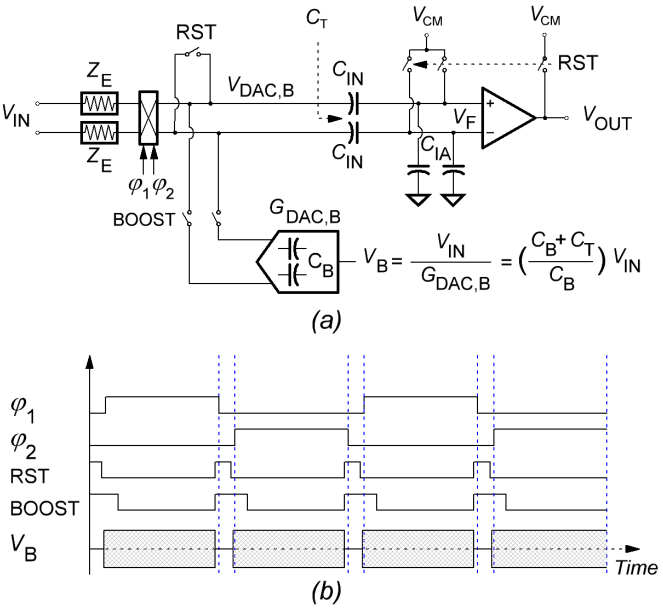

Fig. 6 (a) Proposed impedance booster module, with (b) timing diagram.

multiplexed signal band beyond the amplifier 1/*f* noise corner frequency. Then the signal is amplified, and the ADC samples the signals at an oversampled rate $\alpha \times f_{Clk} = 2 f_{Chop}$.

Normally, a down-modulating chopper is inserted after the neural amplifier, then followed by an analog LPF to attenuate the upmodulated flicker noise. Unfortunately, this technique is not valid in the case of a TDMA scheme because the analog LPF will distort the amplified multiplexed signal.

Instead, the down-chopper is moved to the digital domain after the ADC, resulting in a down-chopped (but not demultiplexed) signal at node V_D in Fig. 5. Since no low-pass filtering has occurred yet, flicker noise is still present in this signal. To attenuate this flicker noise, a resettable moving average (RMA) filter acting as a LPF averages α-input samples to node $V_{M,AP}$, afterwards, the filter is reset for the next channel frame.

Unfortunately, with an open loop configuration neural amplifier, its input referred offset, V_{OS}, is expected to saturate the output of the amplifier. Without a chopper, the static input referred offset is automatically removed by the DSP module via the proposed EOV/LFP filter in Fig. 2. However, a chopper will up-modulate the offset and the feedback loop will fail to attenuate it. To solve this issue, a digital integrator, shown in green in Fig. 5, is added to the loop to remove the amplifier input referred offset. The additional loop is composed of an integrator that is used as an LPF, and an attenuation digital shift-right parameter *k* that controls the cutoff frequency of the filter.

The proposed chopping technique reduces overall IRN with an additional cost of power consumption required in the amplifier BW extension, the higher ADC sampling speed, and the higher digital clock with factor α. With the proposed power savings in the EOV/LFP and feedback modules, chopping becomes more attractive to further attenuate the system IRN.

D. Impedance Booster Module

It is well known that chopper-stabilized neural recording systems suffer from reduced input impedance as a cost for reducing flicker noise. In a nominal implementation, the input impedance is estimated to be $Z_{IN} = 1 / 2 f_{Chop} C_{IN}$, where C_{IN} is the input AC-coupling capacitors of the AFE.

Many solutions were proposed over the last decade to boost the AFE input impedance with the presence of a chopper for a single channel system [14], [24]. However, it is very challenging to boost the AFE input impedance when a multiple access scheme is used, since each channel needs its own impedance booster module to detect the amount of input current withdrawn from the electrodes and supply it from the booster module. A brute-force solution, such as the one mentioned, would result in increased overhead circuitry, which would translate into a significant rise in per-channel power and area. Thus, a different approach is required.

Fig. 6(a) shows the proposed impedance booster module. Here, the electrodes are modeled to have an impedance of Z_E, and the timing diagram in Fig. 6(b) shows non-overlapping chopper clocks $\varphi_{1,2}$. The total equivalent input capacitance of the analog front end (AFE) is denoted by C_T. Since the polarity of the input signal V_{IN} keeps changing with choppers, C_T keeps charging on each chopping-phase, and this withdraws transient currents from the input source signal V_{IN} that leads to input impedance degradation.

To increase the input impedance, the capacitance C_T needs to be recharged to V_{IN} prior to re-connecting the AFE to the electrodes. However, this requires the prediction of the input signal prior to its application.

Assuming it is possible to do this prediction, $V_{IN,\,predicted}$ can then be applied to a capacitor C_B, which in practice is a capacitive DAC. The DAC can then pre-charge C_T to the predicted V_{IN} value required. This dictates that the voltage applied to the DAC capacitance C_B to be V_{IN} (C_B + C_T) / C_B. Additionally, the voltage required to the DAC is V_{IN} / $G_{DAC,\,B}$, where $G_{DAC,\,B}$ is the impedance booster DAC gain.

With a high electrode impedance Z_E, the resistivity of the impedance-booster to the AFE input capacitors will be orders of magnitude less that the impedance from the electrodes to C_{IN}. Accordingly, the current will be supplied from the impedance-booster module which will cause the overall AFE input impedance to increase.

The timing diagram waveforms shown in Fig. 6(b) are synthesized by on-chip by the DSP module that operates with a master clock of 10.24 MHz. A reset phase (RST) with active high duration of 48.82 ns is added to avoid unnecessary charge sharing between the DAC and AFE capacitances. The applied boost voltage digital code of the DAC (V_B) is set to zero during reset phase. The BOOST phase allows charges to flow from the DAC to C_{IN} prior to connecting the electrodes to the AFE by $\varphi_{1,2}$. The reset and boost signals slightly overlap the ending of $\varphi_{1,2}$ to ensure that the voltage on each terminal is defined and not floating, whereas the DAC and C_T differential charges are set to zero. The neural amplifier is expected to have a BW much lower than the reset phase duration, hence, the RST switches help in the input and output stages of the amplifier to reach V_{CM} which is exactly half the supply.

The following section explains how $V_{IN,\,predicted}$ is calculated in the digital domain, allowing for this scheme to be employed.

III. Design Architecture

The overall proposed neural recording system block diagram is shown in Fig. 7. The system is composed of an analog module containing an analog multiplexer, a chopper, a 2-pF input AC-coupling capacitor C_{IN}, a fully differential neural amplifier biased by pseudo-resistors, a 10-bit ADC, and two 10-bit DACs for EOV/LFP and an impedance booster. The proposed digital module, introduced in section II, assembles the EOV/LFP filter, the DAC size reduction, and the amplifier static offset remover all together.

A. Noise Considerations

In TDMA systems, the amplifier BW should accommodate for the multiplexed signal BW. Assume that the amplifier is a one-pole system, this gives an amplifier transfer function H(s) = A_v / (1 + (s / ω_{BW})), where A_v is the amplifier gain, and ω_{BW} is the dominant pole setting the GBW. The input step u(t) gives an output step response signal $V_{out}(t) = A_v$ (1 - exp(-t / τ_{BW})) u(t),

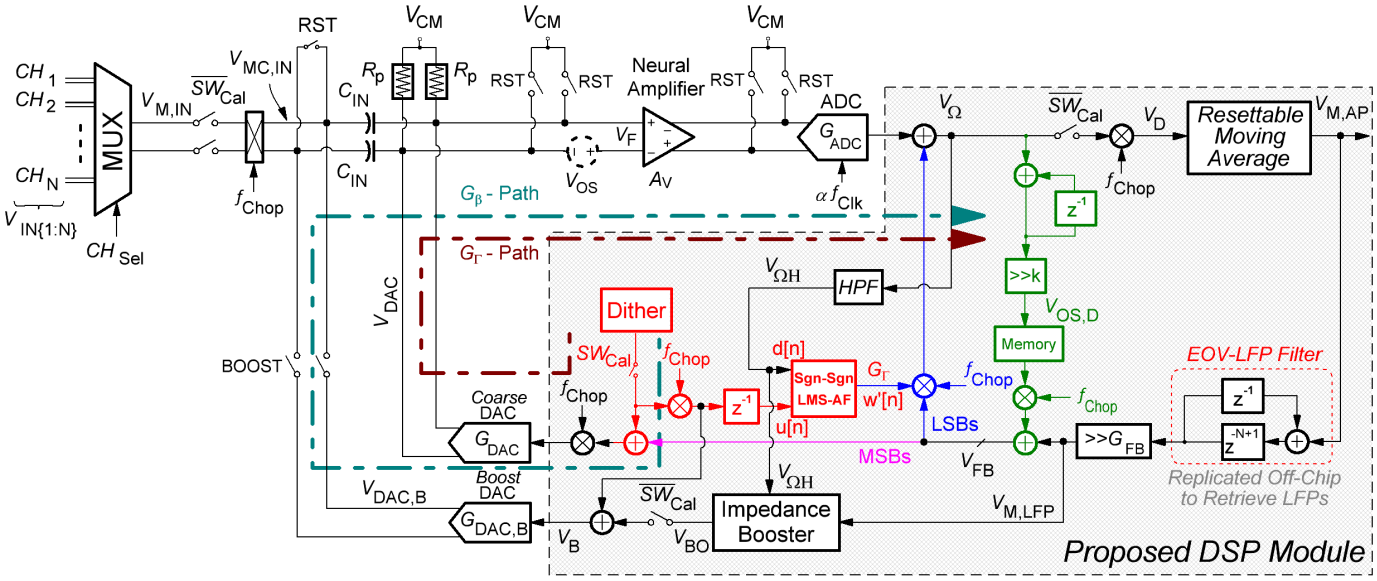

Fig. 7 Proposed neural recording system block diagram.

where $\tau_{BW} = 1/\omega_{BW}$, hence the dynamic error is defined as $\varepsilon = \exp(-t/\tau_{BW})$. Accordingly, $f_{BW} \geq -f_S \ln(\varepsilon) / 2\pi$. If the system includes choppers, then, $f_S = 2 \times f_{CHOP} = 2 \times N \times f_{CH} \times \alpha$, where N=16 channels, f_{CH}=10 kHz, and the oversampling factor is α = 8. Therefore required amplifier BW is $f_{BW} \geq (-N\,\alpha\, f_{CH}/\pi) \times \ln(\varepsilon)$.

The noise of the electrodes should be carefully studied in TDMA systems as the analog multiplexer folds the noise power *N*-times onto the channel bandwidth. This issue can be mitigated by windowed-integration sampling (WIS) [22]. The noise equivalent bandwidth (NEB) of an in-pixel architecture is given by $NEB_{IN\text{-}PIXEL} = \pi\, f_{CH} / 2$, whereas in TDMA Non-WIS systems the $NEB_{NON\text{-}WIS} = \pi\, f_{BW} / 2 = (-N\,\alpha\, f_{CH} / 2) \times \ln(\varepsilon)$. On the other hand, the $NEB_{WIS} = f_s / 2 = N\,\alpha\, f_{CH}$, hence the ratio of the Non-WIS to the WIS multiplexed architecture is equal to the factor $-\ln(\varepsilon) / 2$.

The proposed system integrates the input neural signal current of each channel on the AC coupling capacitors at a rate of f_{chop}. The integrated current is flushed by the reset signal after each sample which creates a windowed-integration Sinc-filter for electrode noise with notches at integer multiples of f_{chop}. This implies that the proposed chopper-TDMA system has higher NEB_{WIS} when compared to non-chopped solutions as in [22] by a factor of α. However, the proposed system contains a digital RMA which reduces the NEB_{WIS} when input-referred by the factor of α, giving $NEB_{WIS\text{-}Input\text{-}Referred} = N\, f_{CH}$. To account for this noise increase, the front-end needs to be designed with sufficiently low thermal noise floor which further motivates the chopping approach.

B. *System Operation Phases*

Initially, the system starts in calibration mode with SW_{Cal} set to logic high, the amplifier static offset module shown in green in Fig. 7 runs first to bring the amplifier out of saturation. The digital LPF *k*-factor is set *k*=15, this sets the filter cutoff almost

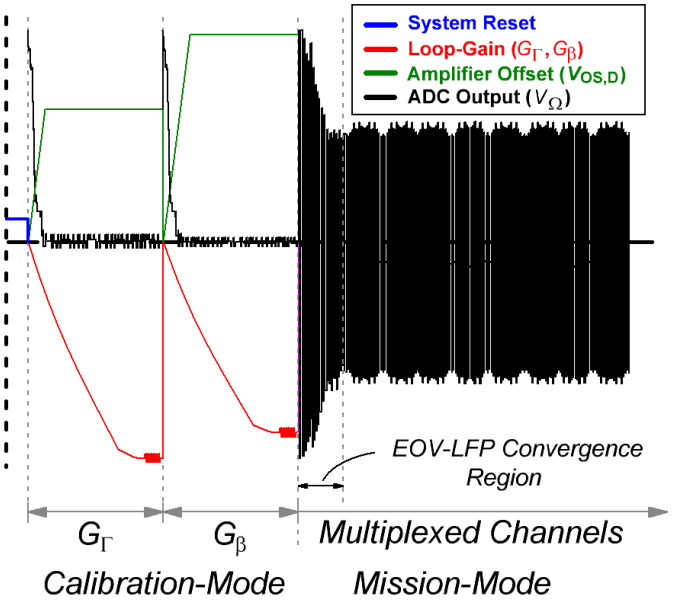

Fig. 8 System transient simulation in calibration and mission modes.

at DC. The DAC MSBs are sufficient to cancel the amplifier static offset regardless of the transient DAC LSBs values, so both amplifier-offset and G_Γ-Path calibrations can run simultaneously. A ±1 dither is injected in G_Γ-Path and the Sign-Sign LMS converges to estimate the value of G_Γ. After 30 ms, the offset and G_Γ are sampled in the digital domain and the static offset calibration module is powered down. Finally, the same dither is reapplied to the impedance booster DAC to determine G_β-path gain as given by

$$G_\beta = G_{DAC,B}\, A_v\, G_{ADC} \tag{4}$$

which is required to predict the input voltage needed for impedance boosting. It is critical to note that the LMS loop

diverges if DC-offset is injected to port *d[n]* [25]. Although the amplifier static-offset remover module works as expected, it is noted that in rare situations the sampled offset value can shift by ±1, which causes a small DC shift in the digital domain. Accordingly, a dedicated high-pass filter (HPF) is used to remove the static DC offset from V_{Ω} and exports $V_{\Omega H}$ to the LMS input node d[n].

Fig. 8 shows the system transient signals after the master reset is set to logic low. Initially, the ADC output is saturated due to the amplifier static offset. The calibration mode starts with G_{Γ}-Path and the amplifier offset calculation $V_{OS,D}$. The amplifier quickly recovers from saturation, and the injected dither amplitude passes to the LMS algorithm for G_{Γ} estimation. Afterwards, G_{β}-path calibration starts, and the amplifier offset needs to be recalculated so that the impedance booster operates with the amplifier out of saturation. All calibrations are finished in 60 ms, the system then switches to mission-mode for neural signal recording by setting SW_{Cal} to logic low. The ADC oversamples each channel α = 8-times before switching to another channel. The proposed EOV/LFP filter starts to converge, Fig. 8 shows the ADC starts at saturation due to EOV, then the multiplexed signals are recovered shortly afterwards. The AP and LFP signals are recovered off-chip; a 10-bit $V_{M,AP}$ signal is exported to an external computing unit. AP signals are directly retrieved by digitally demultiplexing $V_{M,AP}$, and $V_{M,LFP}$ signal is passed through a replica of the proposed EOV-LFP filter off-chip, then demultiplexed to retrieve the LFP recordings. In this work, both $V_{M,AP}$, and $V_{M,LFP}$ are exported to avoid using off-chip logic.

C. *Impedance Booster Operation*

The impedance booster placeholder block shown in Fig. 7 is illustrated in more detail in Fig. 9(a). The module transforms the single-channel impedance booster shown in Fig. 6(a) to TDMA version. The module is fed by two signals, $V_{\Omega H}$ and $V_{M,LFP}$. $V_{M,LFP}$ is either delayed by N-1 clocks or passed to a multiplexer that is controlled by a flag "First Sample" (FS), $V_{M,LFP}$ is chopped and multiplied by G_{Γ}. The summation of both paths is then attenuated by a factor -1/G_{β}.

As previously illustrated in Section 2D, the main goal of the impedance booster is to pre-charge node $V_{DAC,B}$ to a voltage close to $V_{M,IN}$ in an ideal case. With the knowledge of the current ADC output signal $V_{\Omega H}$, the input voltage is used to predict $V_{DAC,B}$. However, the ADC signal $V_{\Omega H}$ is modified compared to the ideal input signal $V_{M,IN}$ since EOV/LFP are subtracted from it via the differential amplifier. Hence, the ideal input multiplexed signal can be written as,

$$V_{\Omega H} = V_{M,IN} A_v G_{ADC} - G_{\Gamma} V_{FB} \quad (5)$$

With the knowledge of eq. (3) and (4), $V_{M,IN}$ can be written using eq. (5) as

$$\frac{V_{M,IN}}{G_{DAC,B}} = \frac{V_{\Omega H} + G_{\Gamma} V_{FB}}{G_{\beta}} \quad (6)$$

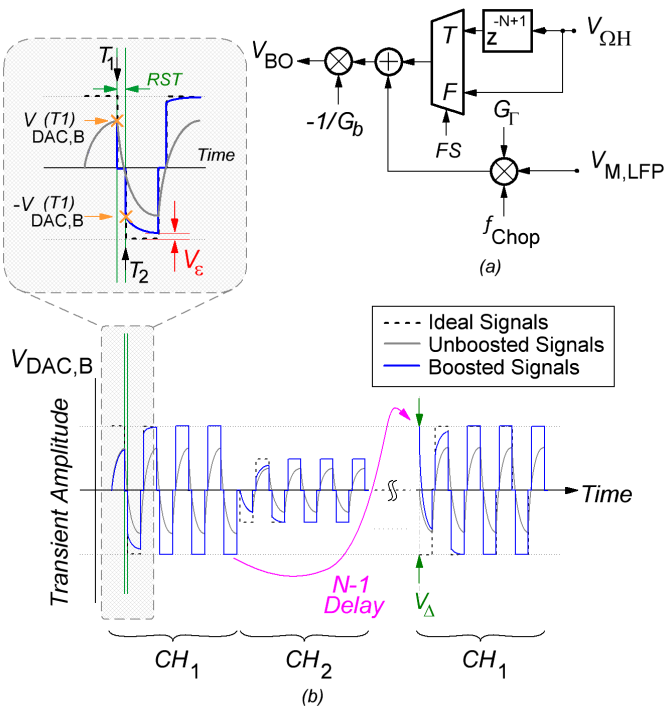

Fig. 9 (a) Proposed impedance booster block diagram, (b) Transient signal example showing the operation of the proposed impedance booster.

From Fig. 6(a), one can note that left-hand term of eq. (6) is exactly what is required to boost the input signal of the proposed neural recording system. Meanwhile, all the right-hand term of eq. (6) are known at every ADC sample. Since the system receives input chopped signals, this dictates that each sample is roughly equal to a (-1)-multiplication factor of the previous sample within a channel frame.

Fig. 9(b) shows an example of the impedance booster in operation with the proposed TDMA neural recording system. If the input signals are un-boosted, then the signal will experience a severe attenuation at the input of the AFE as shown in the transient signal example. When the booster first engages, the FS flag is set to logic zero, and the booster stores the maximum signal marked by the orange arrow at T_1. The booster then multiplies the stored signal by -1 and feeds it back the booster DAC at T_2, then stores the new value, and so on. When the channel frame ends, the booster restores the input signal and saves the last sample value by propagating through an N-1 delay. Assuming that the ADC delays the input by 1-Clk cycle, the overall signal sees N-delay channel-clock units. When the same channel is recorded again, the FS flag is set to logic one, this passes the stored value as the last known good amplitude of the channel.

Since each channel is effectively sampled at a Nyquist rate of 20 kSps, neural signal components with high frequencies can cause V_{Δ} to be as large as twice the ideal signal amplitude after N-delay channel-clock units. Fig. 9(b) shows the worst-case scenario in CH1 where a neural signal plus EOV of a maximum signal amplitude 60 mV is injected with the highest frequency of 10 kHz. After (N-1) unit delays, the booster injects a signal of 200% error. Assuming an electrode with a maximum

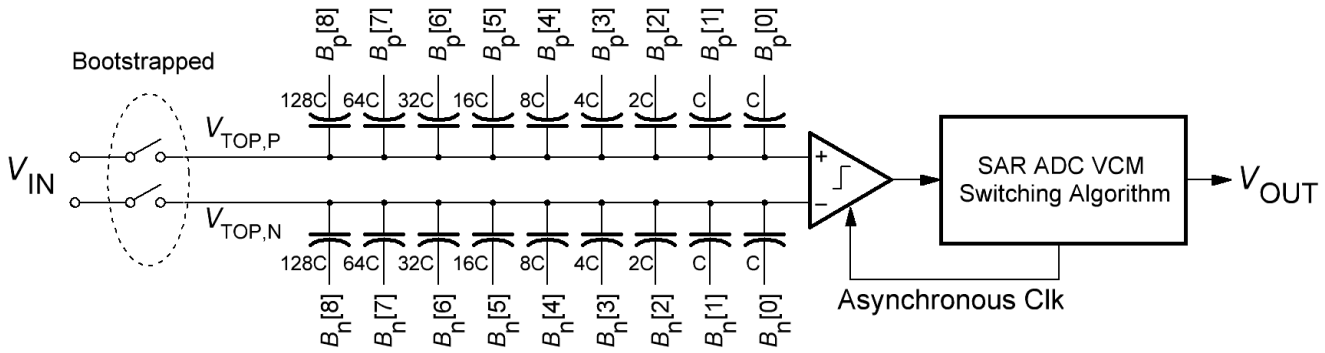

Fig. 10 SAR ADC block diagram with common mode switching algorithm.

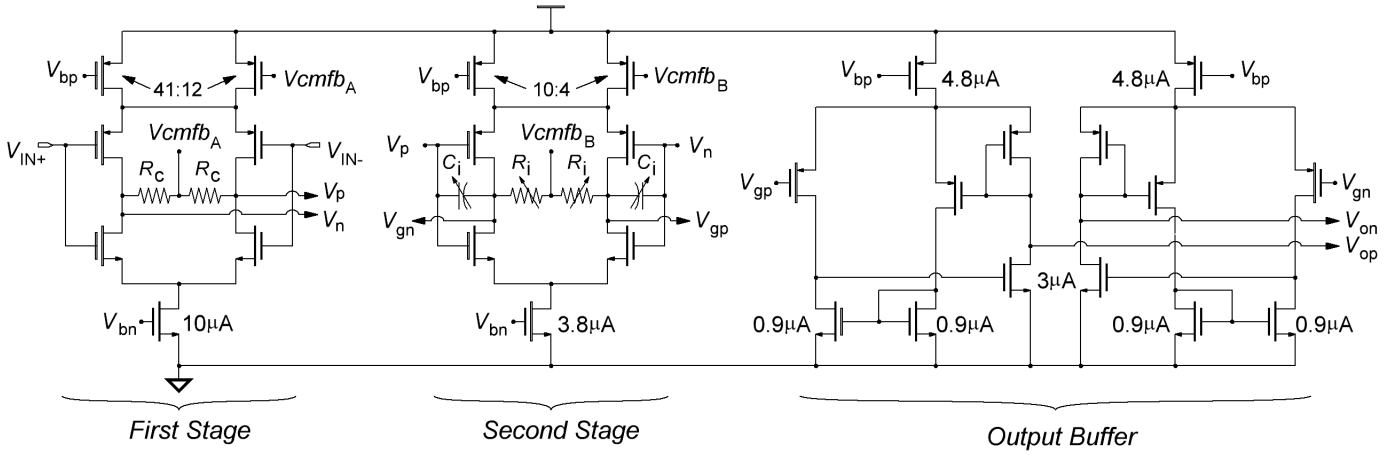

Fig. 11 Two-stage neural amplifier circuit topology with a low-gain-error self-biased unity-gain output buffer.

impedance of 100 kΩ [26], in addition to having an AFE input capacitance 2 pF, the AFE input impedance is ~195 kΩ, given a chopping clock frequency of 1.28 MHz. Hence, in the first cycle the signal approximately undergoes a potential division between the electrode and the AFE impedances which is >±66%. Subsequently, the impedance booster module starts pre-charging of the signal in the appropriate direction, following an RC-charging equation wherein R signifies the electrode resistance and C represents the AFE input capacitance. Post α-samples, the impedance booster reinstates the signal.

Since there are a few samples among the α-samples with errors V_Δ, the resettable MA will average all α-samples with errors larger than 10-bit resolution (i.e: > 0.1%). To mitigate this problem, a digital checker module that is implemented inside the resettable MA filter compares the last sample of the channel frame to the rest of the α-samples. If the sample has error V_ε approximately larger than 5%, then it gets discarded and replaced instantly by the last channel frame sample. This creates a tradeoff between the input impedance and the noise attenuation of factor $\sqrt{\alpha}$ to become $\sqrt{\alpha - \rho}$ where ρ is the number of discarded samples. The higher the electrode impedance or AFE input capacitance become, the higher errors are observed between the α-samples.

IV. Circuit Implementation

The AFE of the proposed neural recording system consists of four main blocks: 1) the analog multiplexer, 2) the neural amplifier, 3) the ADC, 4) the feedback and impedance boosting DACs. The multiplexer and both DACs are implemented with the topologies discussed in [15], where each DAC is composed of a charger-distribution topology of 10-bits. The analog multiplexer IRN and cross-talk are negligiable as discussed in [15].

A. SAR ADC Topology

Fig. 10 shows an asynchronous 10-bit successive approximation register (SAR) ADC block diagram implemented in the proposed neural recording system. The designed SAR ADC uses a common mode-based switching algorithm [27]. However, top-plate sampling is chosen instead of bottom to reduce the number of switches and optimize the ADC overall area. The input sampling switches use the bootstrapped topology discussed in [28] to reduce non-linearities. The digital controller algorithm is synthesized by a standard library cell to control 2^8-unit capacitors in the DAC network, each is implemented by a 2.39fF MOM capacitor, leading to a small 0.62 pF load capacitance. A StrongArm latch

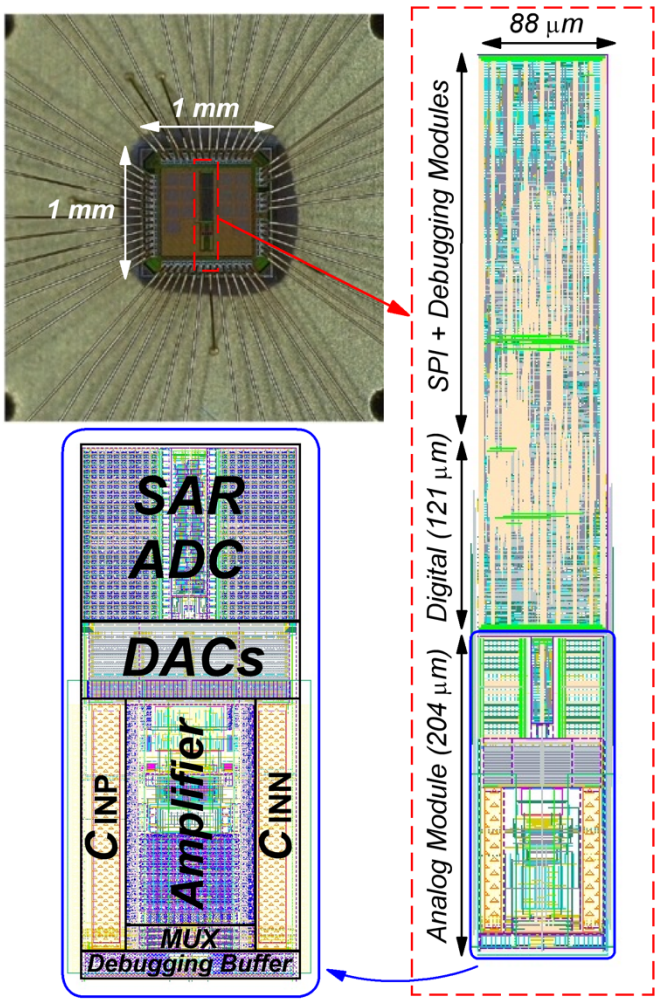

Fig. 12 A microphotograph of the proposed neural recording system wire-bonded IC with modules annotations.

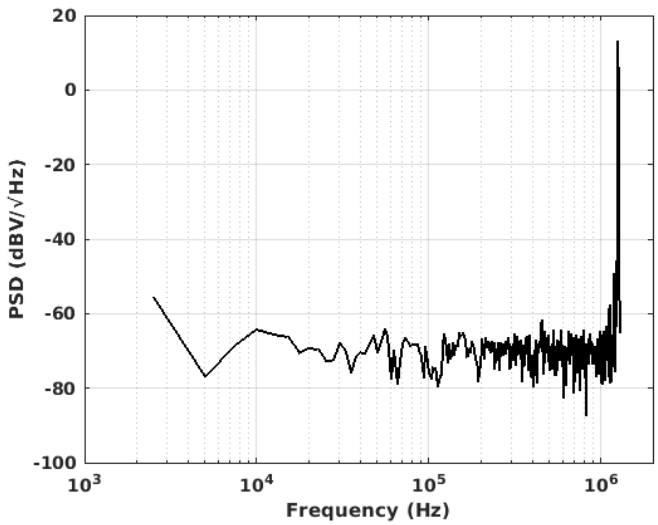

Fig. 13 PSD of the SAR ADC with a sinusoid full-scale input test signal.

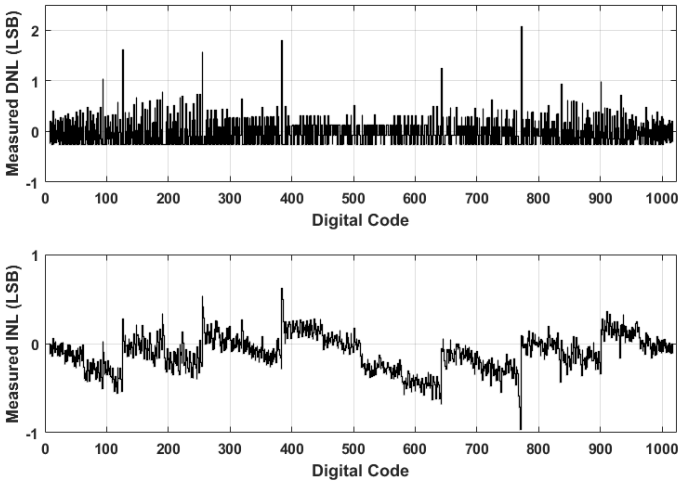

Fig. 14 Measured INL and DNL of the SAR ADC.

comparator topology discussed in [29] is implemented as the main SAR ADC comparator. The overall ADC active area is 86.76 μm × 70 μm.

B. Neural Amplifier Circuit Topology

Fig. 11 shows the designed neural amplifier circuit topology. It consists of a two-stage complimentary-input CMOS amplifier discussed in [30], [15]. The input CMOS devices are biased by pseudo-resistors in the Tera-Ohms range. Hence, with coupling capacitors of 2 pF, the high-pass poles are in the milli-Hertz range across all corners.

To prevent latching during the startup process and minimize stability concerns caused by high loop gain, the current sources in the first and second stages are partitioned into current tails and bleeders. The second stage have variable Millar-capacitors and resistors to adjust the gain-bandwidth (GBW) if needed after fabrication [15].

With a SAR ADC of load 0.62 pF, a self-biased unity-gain buffer with low gain error is used in the output stage [31], this helps the amplifier to operate with the desired BW. The required practical BW should be at least $f_{BW} \geq -f_S \ln(\varepsilon)/2\pi \approx 1.1 f_S$, where the dynamic settling error $\varepsilon \leq 0.1\%$, and f_S is the signal BW [16]. Since f_{CH} = 10 kHz, and N = 16 channels are implemented, then the multiplexer is expected to run at a clock sampling frequency of $f_{CH\text{-}Sel}$ = 2 N f_{CH} = 320 kHz to satisfy Nyquist criterion. Additionally, a chopper clock f_{Chop} = 1.28-MHz up-modulates the entire multiplexed band beyond the worst-case 1/f noise corner frequency. Accordingly, the neural amplifier is expected to amplify a signal of BW f_{BW} = 2.56 MHz, this dictates f_S = 1.1 f_{BW} = 2.81 MHz. If the impedance booster module is engaged, the chopper waveforms have a smaller pulse width of 341.796 ns as shown in Fig. 6(b), as the reset phase width is 48.82 ns. This means that the signal BW is now larger where $f_{BW,\,With\text{-}Booster}$ = 2.92 MHz. Consequently, the required amplifier BW increases to f_S = 1.1 $f_{BW,\,With\text{-}Booster}$ = 3.22 MHz.

V. Measurement Results

The neural recording module was fabricated in 65-nm 1p9m low-power (LP) CMOS technology. Fig. 12 shows a microphotograph of the fabricated 1 mm × 1 mm die. The active area of the digital module is 121 μm × 88 μm, and the analog module is 204 μm × 88 μm. Accordingly, the per-channel area

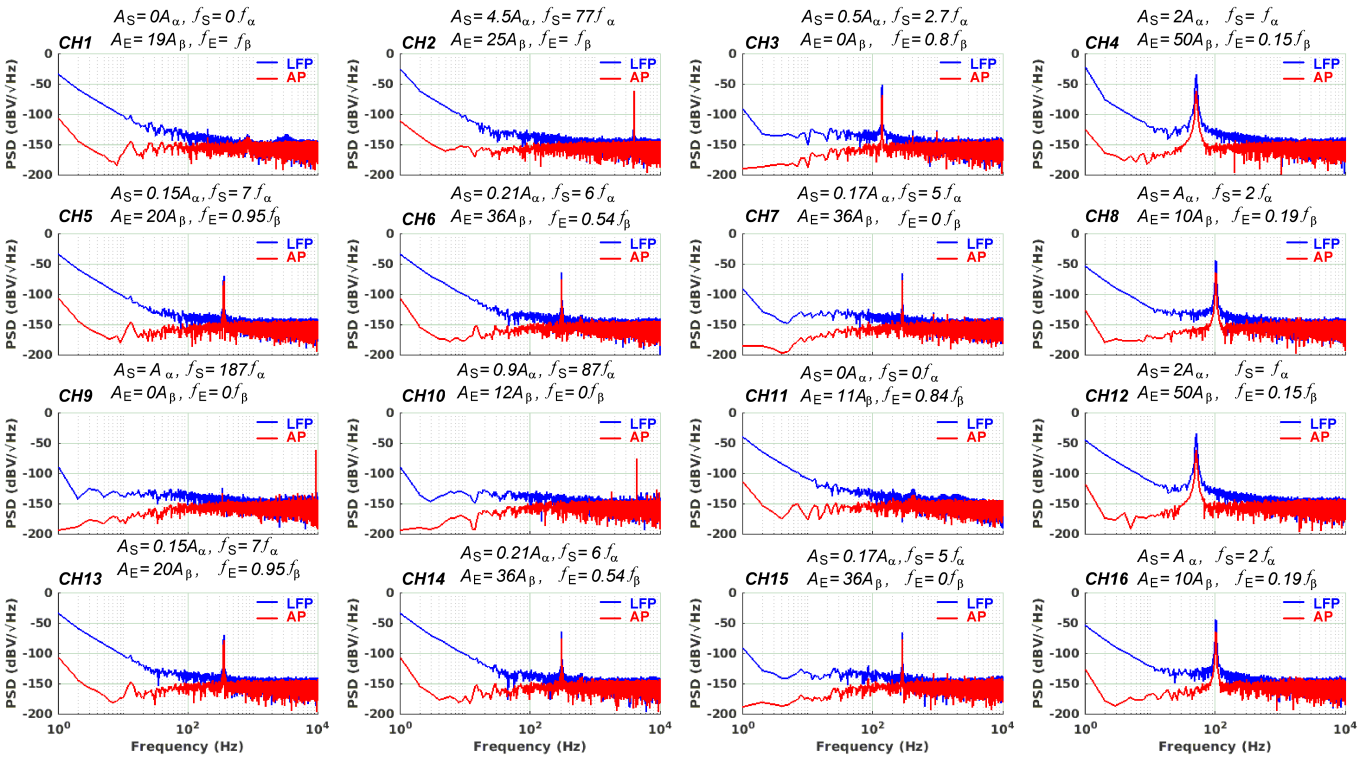

Fig. 15 PSD measurement results of the proposed 16-channel neural recording system with simultaneous injected sinusoid input signals. All injected signals are factors of: A_α = 1 mV, A_β = 1 mV, f_α = 50 Hz, f_β = 0.1 Hz. The signal amplitude is annotated by A_S, the electrode offset is A_E, the f_s is the signal frequency, and f_E is the electrode offset frequency. The PSD plots are input-referred signals to the AFE input ports; the output signal codes are divided by the ADC and amplifier gains ($2^{10}\times199.5$).

is 0.001787 μm^2. The analog and digital modules are supplied by VDD of 1.2 V, and the total current consumption for all 16 channels is 75.6 μA. The digital module consumes 28.4 μA from a 0.9 V supply, whereas the amplifier, the ADC and the DACs consume 25.79 μA, 17.05 μA, 4.36 μA, respectively, from a 1.2 V supply. The lowest common mode rejection ratio (CMRR) is 67.2 dB with ±50 mV injected EOV. Without choppers, the CMRR is degraded to 60.4 dB. The lowest measured power supply rejection ratio (PSRR) is 68 dB.

The SAR ADC runs at a 2.56 MSps speed, Fig. 13 shows the 2048-FFT points power spectral density (PSD) of a 1.03 Vpp injected full-scale test signal at 1.24625 MHz. The measured SNR is 58.31 dB and SNDR is 56.83 dB resulting in ENOB 9.1 bits. Fig. 14 shows the SAR ADC measured integral non-linearity (INL) and differential non-linearity (DNL).

A 2048-FFT point PSD measurement of all 16 channels are measured for LFP and AP bands in Fig. 15. Due to limited number of IC pads, the inputs of channels (4, 12), (5, 13), (6, 14), (7, 15), (8, 16) are shorted on the pads of this test IC. CH1 is only injected with an EOV signal to measure the noise floor of the system, which is found to be to 2.07 μVrms for the AP band, and 2.4 μVrms for the LFP band. The lowest measured EOV attenuation is 54 dB with ±50 mV injected EOV.

The measured input impedance for the fastest injected signal in CH9 with frequency 9.3066 kHz is measured to be 176 kΩ without the impedance booster circuit, and 7.25-MΩ with impedance boosting. The noise floor PSD is measured for this channel to be 2.19 μVrms for AP band, the increase indicates

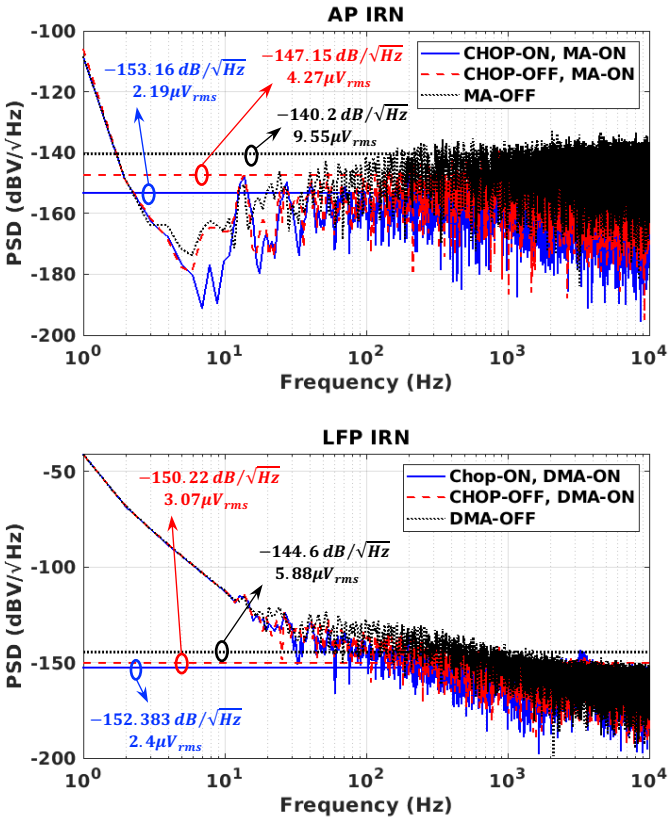

Fig. 16 CH1 measured PSD for different chopping and MA-filter modes of operation.

that there was at least one dropped sample out of α = 8 samples on average. With modern microelectrodes, such as those based

TABLE I
PERFORMANCE SUMMARY OF DIFFERENT NEURAL RECORDING ARCHITECTURES

Reference Author Conf./Journal - Year	[13] MULLER JSSC 12'	[23] HUANG SSCL 18'	[17] UEHLIN TBCAS 20'	[36] WENDLER JSSC 22'	[15] FATHY JSSC 22'	[18] X. HUANG JSSC 22'	[35] X. YANG JSSC 23'	**THIS WORK**
Architecture Type	DC-Coupled In-Pixel	VCO-Based ADC	TDMA	2-Step ΔΣ-ADC	TDMA	TDMA ΔΣ-ADC	Δ-ΔΣ	**TDMA**
Technology (nm)	65	65	65	180	65	22	22	**65**
Channel Area (mm^2)	0.013	0.01	0.0023 + Filt [a]	0.00462	0.00248	0.001[b]	0.0045	**0.00179**
Digital Area % Ratio	< 20% [c]	42%	<9%	58%	68%	11%	29%	**38%**
Number of Ch.	2	1	64	8	16	256	128	**16**
IR Noise AP (μV_{RMS})	4.9[d]	-	-	11.83	2.6 [e]	-	7.71±0.36	**2.19 [d]**
IR Noise LFP (μV_{RMS})	4.3[d]	2.2	1.66	9.21	2.4 [e]	1.55	11.9±1.13	**2.4 [d]**
Gain (dB)	32	-	60	-	48	-		**45**
BW (Hz)	1-10000	1-500	1-1000	0-10000	1-10000	1-500	0.1-10000	**1-10000**
Channel Power (μW)	5.04	3.2	2.98	14.62	3.38	1.61	6.02	**5.1**
PSRR (dB)	64	65	82	77.2	79	84	-	**68**
CMRR (dB)	75	77	76	-	66	98	-	**67.2**
NEF	5.99	8.7	2.21	13.4	1.83	3.85	8.29	**1.8**
Power Supply (V)	0.5	0.6	0.5/2.5	1.8	1/1.2	0.8	0.8	**0.9/1.2**
Input Impedance (MΩ)	-	>500	92	-	28	43[f]	∞	**7.6**

(a) Off-Chip decimation filter (Area not accounted for).
(b) Requires an actively multiplexed electrode array.
(c) Estimated Area Ratio.
(d) LFP noise bandwidth: DC-0.3 kHz, AP noise bandwidth: 0.3-10 kHz.
(e) LFP noise bandwidth: 1.25-0.39 kHz, AP noise bandwidth: 0.39-10 kHz.
(f) Estimated at electrodes

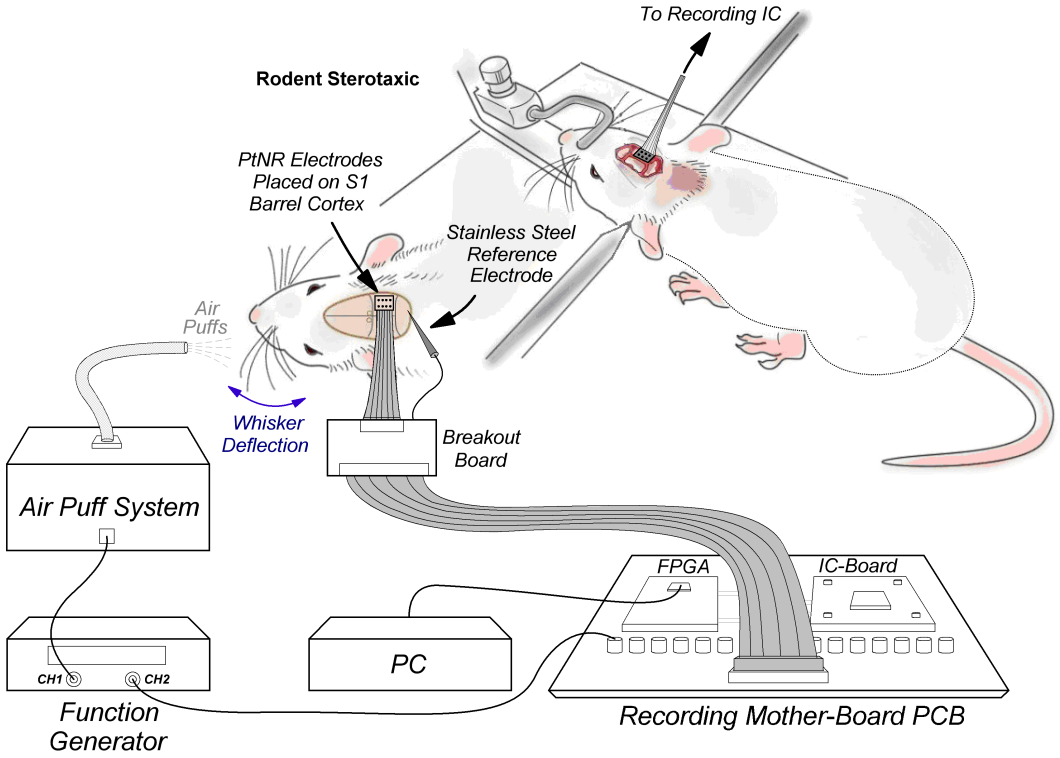

Fig. 17 Schematic illustration of the in-vivo experimental setup showing a Sprague-Dawley rat with the proposed neural recording AFE connected to PtNR electrodes placed on its S1 barrel cortex.

on thin-film materials such as parylene C, the electrode impedances can be as high as 100 kΩ [26]. Accordingly, with the proposed AFE impedance booster, the worst attenuation factor on the AFE interface is 0.986. The lowest SNR, SNDR and ENOB are measured for CH9 to be 52.14 dB, 51.82 dB, and 8.31-bits, respectively. The active area overhead of the proposed impedance booster is only 7.1% of the entire system.

Fig. 16 shows the measured results of AP and LFP in CH1 with different chopping and MA-filter modes. When both chopping and moving-average modules are ON, the PSD noise floor for AP is 2.19 μVrms. When the chopper is turned OFF and MA-filter is ON, the noise floor rises to 4.27 μVrms. Finally, if the MA-filter is switched off regardless the state of the chopper, the noise floor increases to 9.55 μVrms. The same test is repeated

for the LFP band, and the measured PSD noise floor is 2.4 μVrms, 3.07 μVrms, 5.88 μVrms, in the same test order. With a ±50 mV EOV applied, the proposed system achieves a total noise reduction of 2.4× and 4.3× in LFP and AP bands, respectively. The AP band experiences a higher reduction since the 1/*f* noise over the Sinc-modulated multiplexed waveform integrated over the AP BW results in larger cumulative noise impact when chopping is disabled.

Table I shows the proposed system performance summary compared to the state-of-the-art systems. The proposed neural recording system per-channel area is 0.00179 mm^2, which is the lowest amongst systems that can record at 10 kHz bandwidth, and the lowest with fully CMOS-integrated multiplexing. Since the system is composed of 38% digital, it is highly scalable with newer node technologies. The proposed system achieves 1.4× channel active area reduction and 1.2× noise reduction in AP band when compared with [15], while maintaining a state-of-the-art NEF amongst high-density neural recording front-ends. While the power consumption increased over with [15] due to the oversampling of the multiplexed signal due to utilizing choppers to lower the IRN and the per-channel area, the corresponding reduction in noise, which is important in many applications, ultimately maintained the NEF.

Fig. 17 shows a schematic illustration of the *in-vivo* experimental setup for testing and benchmarking the recording capability of the proposed AFE. A female Sprague-Dawley rat is placed on a stereotaxic, and the proposed AFE is connected to a breakout board to interface with the neural electrodes. An Airpuff system and a function generator are connected to inject periodic air puffs towards the whiskers of the rat which evokes responses in its primary somatosensory cortex. Fig. 18 shows *in-vivo* recordings of the proposed neural recording system compared to a commercial IC (Intan RHS). The electrodes used in this experiment were built on a thin-film parylene C substrate [32], [33], [34]. The electrodes were fabricated on a 3-µm thick parylene C layer deposited on a 4-inch Si carrier wafer. A 10-nm thick layer of chromium and 250 nm thick layer of gold were then deposited by electron beam evaporation to form the photolithographically defined metal trace connections to the contacts. The electrode contact is a circular 200 µm diameter Platinum Nanorod (PtNR), which has a characteristic impedance of approximately 2 kΩ at 1 kHz *in-vivo.* Typical benchtop and *in vivo* impedance spectra can be found in [26]. A conformal 2.5 µm thick parylene C top passivation was formed using chemical vapor deposition. The acute *in vivo* recordings in this experiment lasted 3 hours. The electrodes, with a 1-mm inter contact spacing, were placed on the barrel cortex of the rat which is responsive to mechanical deflection of the contralateral whiskers. The baseline and two-consecutive stimulation evoked responses were measured sequentially from CH1 and CH2, revealing similar neural high-gamma activity in the LFP band, measured first with the Intan RHS chip (Fig. 18, right), and consequetively with proposed recording system (Fig. 18, left) without displacing the electrode. The average waveform of four trials filtered in the high gamma band are plotted from two channels in each IC and superimposed on the baseline recordings for the same channels. All experiments

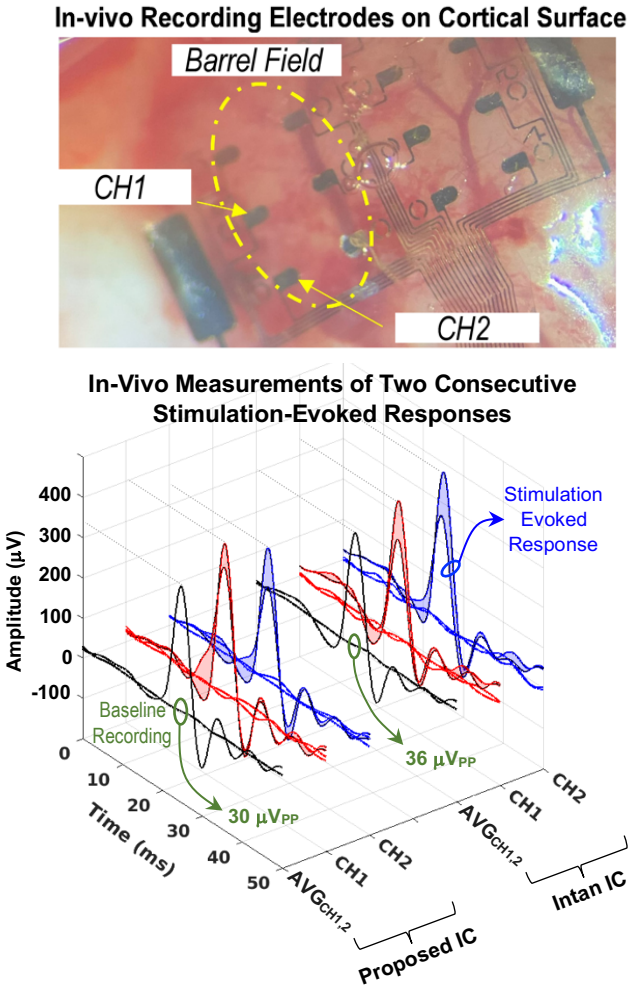

Fig. 18 In-vivo measurement comparison of neural activity of a rat with the proposed IC and a commercial chip (Intan RHS).

were performed under the guidelines stated in the University of California San Diego Institutional Animal Care and Use Committee (IACUC) protocol S16020. The animals were anesthetized prior to surgery using Isoflurane, and constant anesthesia was maintained throughout the course of the experiment using Ketamine. At the end of the experiment, the animal was euthanized with a lethal injection of Sodium Pentobarbital.

VI. Conclusion

This paper presents a TDMA-based neural recording system with novel modules to lower the per-channel area and power consumption. The AFE is based on a chopper-stabilized neural amplifier with a novel impedance booster module that achieves a 39× boosting factor. The proposed neural recorder implements a moving-average filter to lower the amplifier residual flicker noise which affects the system input referred noise (IRN) by a factor of 4.3× for AP band, and 2.45× for LFP band. In addition, no on-chip demodulation is required to extract and remove the EOV artifacts that can easily saturate the AFE. A small size Sign-Sign LMS module replaces the conventional ΔΣ-modulators and fine DACs usage to

completely attenuate the EOV in feedback. The designed neural channel consumes 5.11 μW of power, with 1.8 NEF for AP band, and occupies an area 0.00179 mm^2. The proposed system is verified by comparing it with a commercial IC via *in-vivo* recordings from a rat.

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Nader Sherif Kassem Fathy (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electronics and telecommunication engineering from Ain Shams University, Cairo, Egypt, in 2013 and 2018, respectively, and his PhD degree in electrical and computer engineering from the University of California San Diego (UCSD) in 2024. From 2014 to 2016, he worked as a Teaching Assistant with the Department of Electronics and Communications, Ain Shams University. He was a former Senior Software Development Engineer with the Calibre Research and Development Department, Mentor Graphics—Siemens, Cairo, from 2013 to 2018. He has held two internships with Apple Inc., Cupertino, CA, USA, during the summer of 2020 and 2021 with the Analog Silicon Engineering Group focusing on phase-locked loop (PLL) designs. In 2024, he joined Marvell Semiconductor Inc at Irvine, CA as a staff engineer in analog and mixed signal (AMS) circuit design.

Ritwik Vatsyayan (Graduate Student Member, IEEE) is a PhD student in the Integrated Electronics and Biointerfaces Laboratory at the University of California, San Diego. He earned his B.Tech degree in Electronics and Communications Engineering from the Indian Institute of Technology, Guwahati, and his MS degree in the medical devices and systems track within Electrical Engineering from the University of California, San Diego. His research interests primarily lie in developing safe stimulation paradigms for probing neural networks. His work involves utilizing high channel count, clinically translatable electrodes capable of simultaneous recording and stimulation at ultra-high resolutions.

Andrew M. Bourhis (Graduate Student Member, IEEE) is a PhD student at University of California, San Diego working out of the Integrated Electronics and Biointerfaces Lab. He earned his BS in Electrical Engineering from Tufts University and his MS in Electrical Engineering with a focus on Medical Devices and Systems at University of California, San Diego. His research focuses on designing active circuits and systems on flexible substrates for high channel count neural interfaces, focusing on addressing the interconnect bottleneck that has held back neural interface channel counts for decades.

Shadi A. Dayeh is a Lebanese American Neurotechnologist who pioneered human brain recordings with multi-thousand channels since 2019 and is an ECE Prof. at UC San Diego. He is an awardee of the NIH Director's New Innovator Award, NSF CAREER Award, ISCS Young Scientist Award and was a J.R. Oppenheimer Fellow at Los Alamos.

Patrick P. Mercier (S'04–M'12–SM'17) received the B.Sc. degree in electrical and computer engineering from the University of Alberta, Edmonton, AB, Canada, in 2006, and the S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2008 and 2012, respectively.

He is currently a Professor in Electrical and Computer Engineering at the University of California San Diego (UCSD), where he is also the co-Director of the Center for Wearable Sensors and the Site Director of the Power Management Integration Center. His research interests include the design of energy-efficient microsystems, focusing on the design of RF circuits, power converters, and sensor interfaces for miniaturized systems and biomedical applications.

Prof. Mercier has published over 200 peer-reviewed papers, including 26 ISSCC papers, 34 JSSC papers, and several papers in high-impact journals such as Science, Nature Biotechnology, Nature Biomedical Engineering, Nature Electronics, Nature Communications, Advanced Science, and more. He has received numerous awards, including a Natural Sciences and Engineering Council of Canada (NSERC) Julie Payette fellowship in 2006, NSERC Postgraduate Scholarships in 2007 and 2009, an Intel Ph.D. Fellowship in 2009, the 2009 IEEE International Solid-State Circuits Conference (ISSCC) Jack Kilby Award for Outstanding Student Paper at ISSCC 2010, a Graduate Teaching Award in Electrical and Computer Engineering at UCSD in 2013, the Hellman Fellowship Award in 2014, the Beckman Young Investigator Award in 2015, the DARPA Young Faculty Award in 2015, the UC San Diego Academic Senate Distinguished Teaching Award in 2016, the Biocom Catalyst Award in 2017, the NSF CAREER Award in 2018, a National Academy of Engineering Frontiers of Engineering Lecture in 2019, the San Diego County Engineering Council Outstanding Engineer Award in 2020, the ISSCC Author Recognition Award in 2023, and the ECE Teacher of the Year award in 2023. He has served as an Associate Editor of the IEEE Transactions on Very Large-Scale Integration (TVLSI), the IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), and the IEEE Solid-State Circuits Letters. He is currently a member of the Executive Committee of ISSCC, and has served on the technical program committees for ISSCC, CICC, and the VLSI Symposium. Prof. Mercier was the co-editor of Ultra-Low-Power Short Range Radios (Springer, 2015) Power Management Integrated Circuits (CRC Press, 2016), and High-Density Electrocortical Neural Interfaces (Academic Press, 2019).