A 2.5–20 kS/s In-Pixel Direct Digitization ECoG Front End With Submillisecond Stimulation Artifact Recovery

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***Abstract*— Neural stimulation is used routinely to diagnose and treat neurological disorders. The stimulation artifacts are, however, problematic for closed-loop neuromodulation therapy, which dynamically adjusts the electrical stimulation parameters based on real-time feedback from the recorded neural activity because they can cause saturation or prolonged recovery times in traditional recording front ends. This article presents a per-pixel second-order ΔΣ analog-to-digital converter (ADC) for direct digitization of neural signals, which addresses the stimulation artifact recovery time in voltage-controlled oscillator (VCO)-based quantizers with a fast-recovery, overrange-detecting phase quantizer. The ADC uses a pseudo-virtual ground feedforwarding (PVG FF) technique and a complementary input G_m-C filter with per-pixel decimation. It supports four recording modes covering 2.5–20 kS/s through a power-efficient, bandwidth-scalable continuous time ΔΣ modulator. Fabricated in a 180-nm CMOS process, this 300 × 300 μm^2 ADC achieves >250× faster (0.05–0.4 ms) stimulation artifact recovery time, enabling in-stimulation recording. Recording with artifact tolerance was demonstrated through an in vivo whisker barrel rat experiment.**

***Index Terms*— Artifact tolerance, closed-loop, delta-sigma modulation, neural recording, neuromodulation, recovery time, stimulation artifacts, voltage-controlled oscillator (VCO).**

I. Introduction

CLOSED-LOOP neuromodulation is an advanced therapy that uses real-time feedback to adjust neural stimulation, effectively treating neurological disorders such as epilepsy and Parkinson's disease [1], [2], [3], [4]. It is also used for feedback in brain-machine interfaces and neuro-prosthetics for paralyzed people [5], [6] and in localizing functional tissue during brain surgeries [7]. Neural stimulation sends controlled current pulses into specific brain regions to modulate brain activity. Open-loop stimulation can have detrimental side effects, whereas closed-loop systems adapt based on the patient's recorded neural signals, enhancing treatment precision and efficacy with fewer systemic side effects [8].

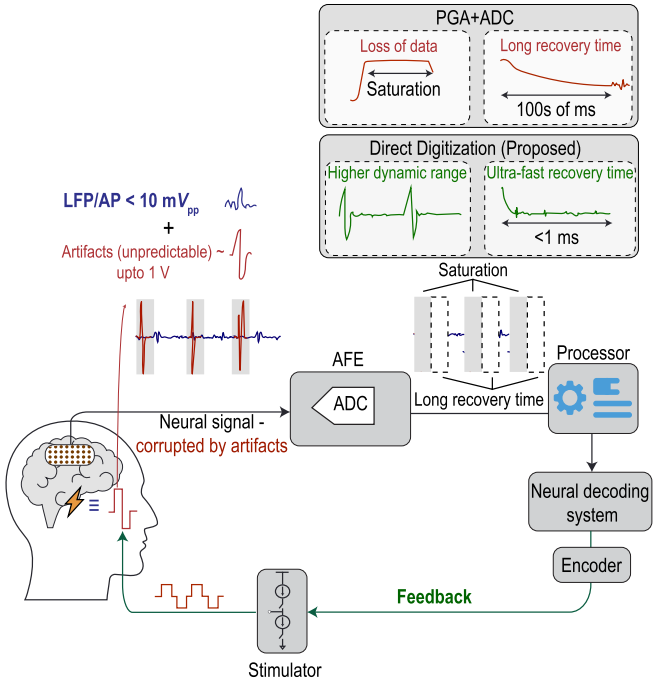

Fig. 1. Closed-loop neuromodulation system illustrating stimulation artifacts.

Fig. 1 shows a typical closed-loop neuromodulation setup. There are several techniques to record neural activity that are classified by the recording location within the brain or on the surface of the scalp. While the design and techniques described in this article can be applied in all neural recording methods, this work focuses on electrocorticography (ECoG), where the electrodes are placed on the pial surface of the cerebral cortex to measure local broadband electrical activity, including local field potentials (LFPs) and extracellular action potentials (APs). These neural signals have spectral content from 1 mHz to 10 kHz with peak amplitudes up to 10 mV_{pp}

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[9], requiring less than 10 μV_{rms} noise from the front end [10]. Recording neural activity has been most commonly accomplished with metal electrodes, which have a finite, nonlinear electrochemical impedance at the electrode-tissue interface. The interface impedance depends on the electrode dimensions but is relatively high at low frequencies due to their capacitive nature (nF range) and becomes nearly resistive above 1 kHz [11]. For capturing low-frequency neural activity and avoiding signal attenuation, the recording front end requires MΩs of input impedance to have a high-pass corner frequency of less than 1 Hz. The neural signals are captured by the analog front end (AFE) and then processed in real-time by a neural decoding system, often using algorithms to detect pertinent patterns or anomalies [12], [13]. This information configures the stimulator to deliver electrical stimulation to the patient accordingly.

Simultaneous recording of neural signals with electrical stimulation presents a technical challenge due to the stimulation artifacts. Electrical stimulation is typically delivered in current mode for precise charge control. With current amplitudes up to ±5 mA and electrode impedances above a few kΩ, the excitation voltages can exceed 10 V [14]. A fraction of this signal may appear as a stimulation artifact at the recording circuit input, marked by large voltage transients coinciding with stimulation pulses, often exceeding the neural signal by more than 100× [15], [16]. The stimulus induces pickup on other electrode channels through capacitive crosstalk between stimulating and recording electrodes, direct conduction paths through cerebrospinal fluid, and/or capacitive coupling to the recording electronics via traces, generating substantial stimulation artifacts at the recording sites. Precise modeling of the artifact is impractical because their morphologies depend on stimulator architecture, current, stimulation waveform, electrode configuration and placement, and patient physiology [17], [18].

This article reports a 4 × 2 array of per-pixel second-order ΔΣ modulators for ECoG (LFP + AP) recording with a submillisecond artifact recovery time, enabling in-stimulation recording. This is achieved using an ac-coupled architecture with a time-based ring-oscillator quantizer featuring fast recovery and overrange detection. The architecture also offers a unique power-efficient bandwidth scaling option. The performance of this chip was demonstrated through an in vivo whisker barrel rat experiment and compared against a commercial chip (Intan RHD2164) [19]. This article extends the work presented in [20].

The rest of this article is organized as follows. Section II discusses prior art, followed by the proposed architecture in Section III. Section IV describes the circuit implementation, and Section V presents measurement results. Finally, concluding remarks are made in Section VI.

II. Prior Art

Advancements in low-impedance, high-density recording grids [21] have paved the way for low-noise neural recording systems with high spatial and temporal resolution. A conventional AFE architecture consists of a high-density neural recording signal path with programmable gain amplifiers (PGAs) and a shared analog-to-digital converter (ADC) [22], [23], [24], [25], [26]. The amplification stage is typically implemented as an ac-coupled instrumentation amplifier (IA) with ∼40 dB of gain, capable of effectively rejecting the tens of mVs of electrode dc offset (EDO) commonly present at the electrode-tissue interface. With an input range of a few mVs, this type of AFE readily saturates during stimulation due to the high gain. The high-pass network at the input, furthermore, requires large on-chip capacitors to achieve a cutoff frequency of less than 1 Hz. Because of this fundamental trade-off with the cutoff frequency and settling time, it takes hundreds of milliseconds to recover from an artifact, leading to critical data loss [Fig. 2(a)]. A dc-coupled AFE with a mixed-signal servo loop reduces area by removing the ac-coupling capacitor, but it still suffers from stimulation artifacts due to its limited input range [27]. Other techniques have been reported to deal with the artifacts, such as blanking the recording during stimulation and adding a discharging circuit to the input [28]; however, with multiple independent, spatially distributed stimulation channels, this incurs significant information loss. Synchronizing the blanking control signal requires precise design regarding its timing and placement relative to the stimulation waveform. Often, this synchronization necessitates incorporating a guard band period alongside the blanking time, which can result in further data loss. Another drawback of this architecture is the need for explicit antialiasing filters to prevent the folding of interference and out-of-band signals into the Nyquist band, which is often neglected in the analysis [29], [30].

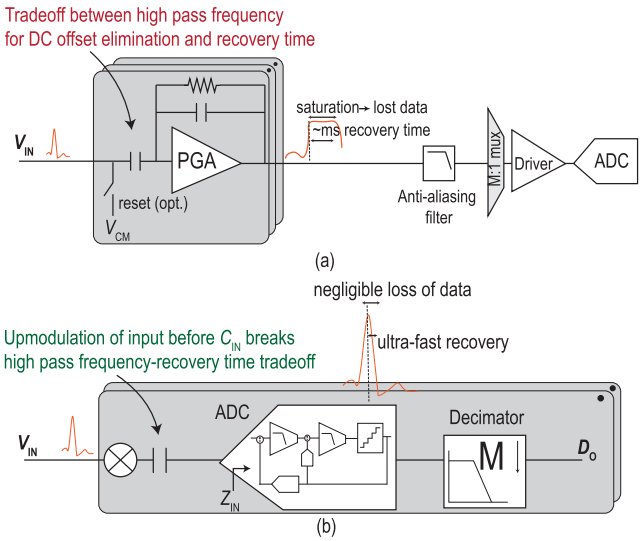
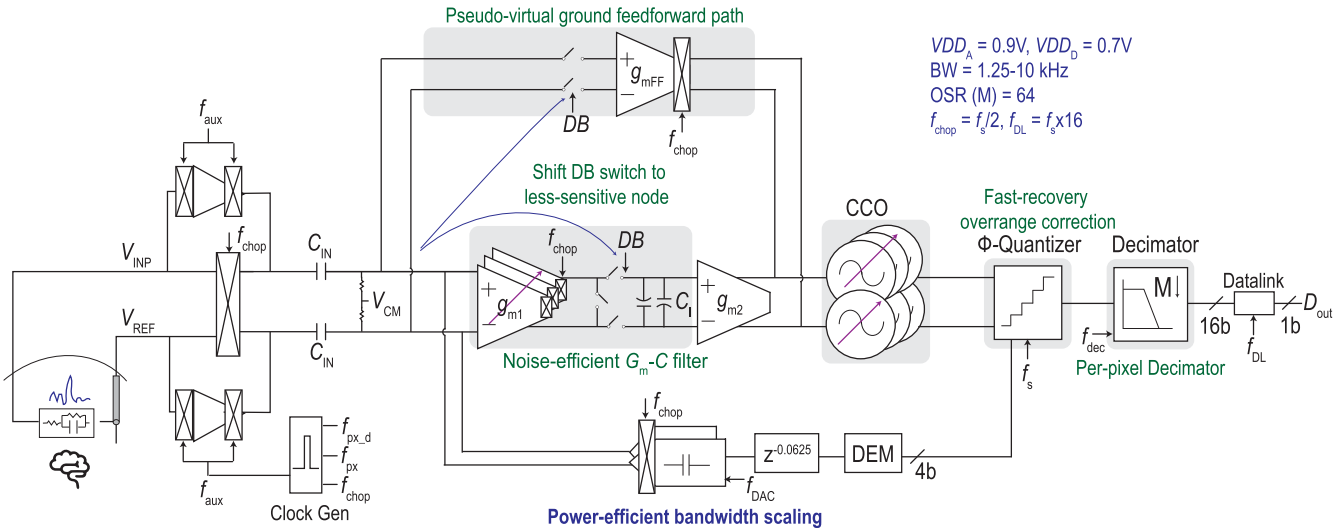


Fig. 2. Comparison of (a) PGA + ADC architecture with and (b) ac-coupled direct digitization architecture in the presence of stimulation artifacts.

Recent advances in direct digitization-based AFEs overcome this artifact-related saturation limitation by forgoing the amplifier and directly connecting the electrode to a high dynamic range (DR) ADC, typically a continuous-time ΔΣ modulator (CT-ΔΣM) [31], [32], [33], [34], [35], [36], [37], [38]. Removing artifacts from a digitized signal requires a wide DR to quantize all signals without saturation. CT-ΔΣMs also benefit from inherent antialiasing filtering, eliminating the



	f_s	BW	$G_{m,1}$	$G_{m,2}$	$G_{m,3}$	K_{CCO}	C_I	C_{DACu}	C_{IN}
Mode 0	160 kHz	1.25 kHz	11.87 µS	0.64 µS	9.5 µS	3.37 MHz/µA	9 pF	3.2 fF	660 fF
Mode 1	320 kHz	2.5 kHz	23.75 µS			6.75 MHz/µA			
Mode 2	640 kHz	5 kHz	47.5 µS			13.5 MHz/µA			
Mode 3	1.28 MHz	10 kHz	95 µS			27 MHz/µA			

Fig. 3. Block diagram of the proposed architecture and key coefficients.

need for power-intensive filters at the front of the signal chain. Different architectures have been explored for stimulation artifact tolerance. Δ-ΔΣ modulators are suitable for high-density arrays for their area efficiency and EDO tolerance [32], [39]; however, these systems either have a low ac input range, making them intolerant to artifacts, or, as in [33], attempt to increase the ac input range but suffer from degraded settling speed due to the feedback integrator and increased distortion at high input levels. A CT-Zoom ADC improves the DR by adapting AFE gain to input signal amplitude but experiences higher noise at low PGA gain settings due to the ADC quantization noise [40]. Incremental ADCs are another area-efficient solution for high-channel-count neural arrays with simpler decimation filters and ease of multiplexing [36]; however, they suffer from poor antialiasing. A dc-coupled architecture ensures a high input impedance, but it comes at the cost of sensitivity to the input common-mode voltage [31], [34]. Lee et al. [31], Jeon et al. [34], and Pochet et al. [41] employ time-based quantizers, which are susceptible to slow recovery/instability during artifacts beyond the input range and are unsuitable for clinical systems unless measures are taken to handle this case.

Fig. 2(b) demonstrates how ac-coupled CT-ΔΣMs break the trade-off between the high-pass cutoff frequency and artifact recovery time by upmodulating the input before the ac-coupling capacitors [41], [42]. EDO and stimulation artifacts are upmodulated along with the input signal, which is subsequently downmodulated within the ADC, while the ADC's input impedance defines the high-pass cutoff frequency. Directly using an ac-coupled CT-ΔΣM for this application, however, has several challenges: slow recovery/instability during artifacts beyond the input range of the time-based quantizer, power and area limitations, and low-input impedance.

III. Architecture

A. ADC Architecture

The proposed ΔΣ ADC architecture is shown in Fig. 3. The ΔΣ modulator is comprised of a second-order loop filter with a 17-level quantizer and has an oversampling ratio (OSR) of 64. It uses the pseudo-virtual ground feedforward (PVG FF) architecture, which allows the modulator to have high linearity and a compact area [43]. The technique feeds forward the error voltage at the PVG node instead of the input with appropriate scaling, linearizing the first integrator by having it only process the quantization noise. This enables the loop to operate with the same dynamics as the standard feedforward-based architecture while eliminating the internal feedback DAC(s) and having the feedforward path process only a small swing, helping with its linearization. The FF path causes signal transfer function (STF) peaking and reduced antialiasing. A maximally flat noise transfer function (NTF) with an out-of-band gain (OBG) of 2.5 was chosen to reduce quantization noise folding through first integrator nonlinearity and reduce sensitivity to coefficient variation.

While time-domain-only ADC architectures, such as voltage-controlled oscillator (VCO)-based ADCs, are popular for their ability to run off a low-supply voltage and process scalability [41], [44], they contend with issues, such as VCO flicker ($1/f$) noise since they cannot be chopped and compromised noise efficiency when used as the first integrator [44]. This system instead uses a G_m-C filter as the first integrator, using chopping to reduce the $1/f$ noise. At low frequencies, chopping also improves the ADC's common-mode rejection ratio (CMRR). The chopping frequency, f_{ch}, is set to half of the sampling frequency, $f_s/2$, to avoid quantization noise folding [45]. The low-frequency noise and offset are

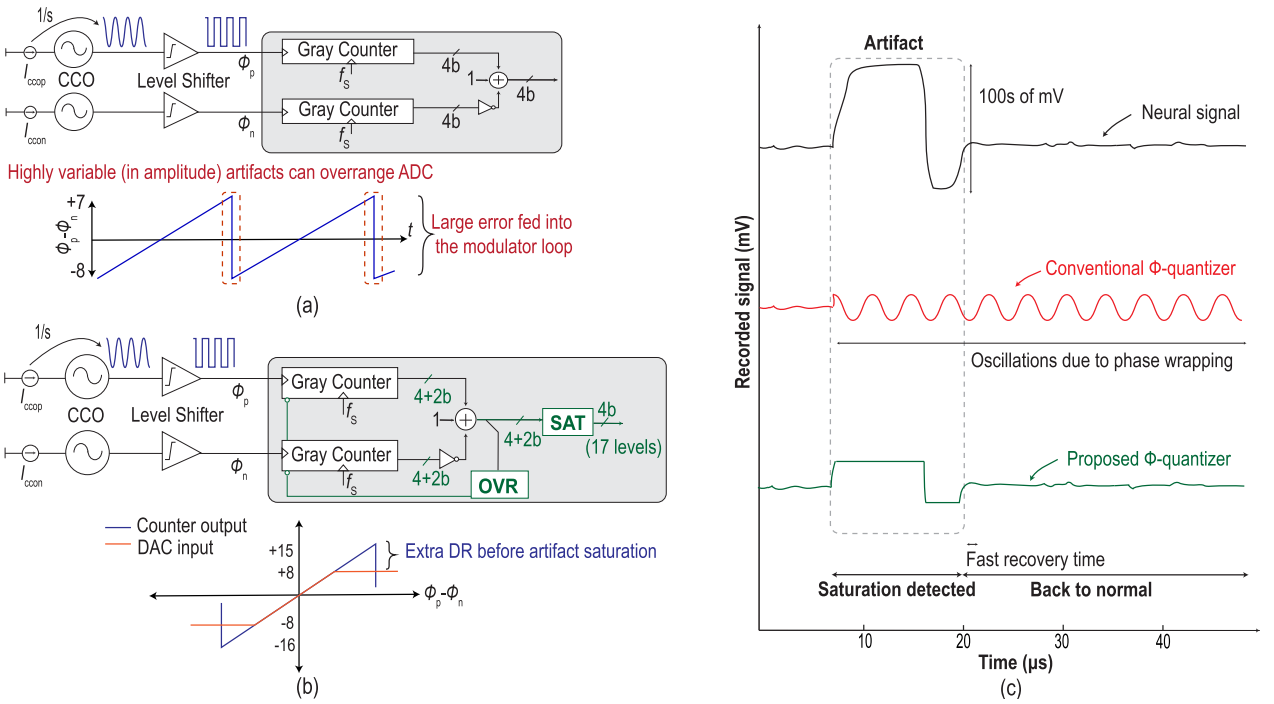


Fig. 4. Details of (a) conventional phase quantizer, (b) proposed phase quantizer, and (c) timing waveforms.

upmodulated to a higher frequency, which goes through the ADC STF and is filtered out by the decimation filter. The second stage is an area-efficient time-based integrator realized by a G_m-current-starved current-controlled oscillator (CCO) with a counter. The outputs of the G_m-C filter, FF path, and capacitive DAC (C_{DAC}) are chopped to ensure correct polarity in the loop.

The CCO's phase is quantified with 6-bit counters, a differencer, and logic that detects quantizer overrange and prevents phase wrapping [41], [44], [46]. This technique ensures ADC stability amid large artifacts that may cause ADC overranging. The 4-bit feedback C_{DAC} is mismatch-shaped with a first-order shaped tree-structured dynamic element matching (DEM) encoder and resampled with a delay of 6.25% of the modulator sampling period (T_s) to account for the quantizer and DEM delay. The ADC output is passed through the decimation filter, which reduces the ADC data rate to the Nyquist rate, f_{dec}, reducing datalink power.

Chopping the C_{DAC} induces large differential-mode chopping artifacts at the high-impedance PVG node due to the sudden switching and settling of the DAC capacitors upon a polarity swap, causing harmonics and quantization noise folding. Deadband (DB) switches suppress the differential chopping artifacts at the G_m input [42]; however, they must be large for low-input-referred noise (IRN) applications and would load the input. For remedying this issue, the DB switches are moved from the sensitive input node to the G_m-C output and the feedforward input and opened for 6.25% of T_s during chopping.

Chopping before the input capacitance reduces the input impedance to the MΩ level, which is too low to interface with small electrodes (that have several MΩ impedances). An auxiliary amplifier precharges the input capacitance after the chopping clock, thus reducing the charge that needs to be supplied from the electrode and increasing the input impedance, Z_{IN}. The input impedance is increased to greater than 30 MΩ using this technique. The input impedance booster was implemented similarly to [15] using buffer duty cycling for power savings. Chandrakumar and Markovic [15] use back-to-back choppers after the amplifiers due to dual chopping frequencies. Since we chop the modulator and the auxiliary amplifiers (f_{aux}) at $f_s/2$, we can combine the switches (M_2 and ϕ in [15]) into a single set of switches, reducing charge injection.

B. Artifact Rejection

In theory, direct digitization offers uninterrupted monitoring by offering a higher DR to accommodate artifacts. As shown in Fig. 4(a), a conventional phase quantizer receives the phase output from a level shifter, which converts the CCO phase output of the integrated G_m current into a rail-to-rail signal. It then quantizes this phase using Gray counters for the positive and negative sides and subtracts the results to obtain the ADC output. The n-bit counters operate with modulo-2^n arithmetic, where the output "wraps around" when reaching $-2^{n-1} < D_C < 2^{n-1} \_ 1$, where D_C is the counter output. The phase difference is thus limited to 2^n arithmetic. With large inputs like stimulation artifacts that can momentarily overrange the ADC, the phase difference at the n-bit counter output wraps modulo 2^n, introducing a large error back into the loop. This results in modulator oscillations leading to phase wrapping-induced instability. Previous work will oscillate indefinitely and require all integrators in the modulator to be reset to restore normal operating conditions, creating a long period of data corruption impractical in closed-loop neuromodulation [38], [41], [43]. Since the signal strength

of these artifacts varies greatly due to external factors like electrode design and human physiology, increasing the ADC's DR beyond a certain point becomes inefficient.

Fig. 4(b) shows the implementation of the proposed fast-recovery, overrange detecting phase quantizer. We introduce a saturation detector and expand the counter depth by two additional bits. One extra bit would have been sufficient to detect saturation and reset the counters, but using just one extra bit would have reduced the no-overload range of the ADC due to clipping. In practice, a few decibels of backoff are required to avoid this. A voltage quantizer does not have the two complement wrapping exhibited by the CCO quantizer. To address this issue, we add two additional bits: the first bit allows the second integrator to exceed the clipping point by 6 dB and extends the modulator's no-overload range. The second bit provides the necessary DR for modulator reset without allowing a phase wrap at the difference, which will destabilize the modulator. The circuit for the added bits is clocked at a fraction of the CCO frequency, f_{CCO}, and thus, requires negligible additional power. Overload recovery is nearly instantaneous after an artifact, as the counter resumes counting once the input returns to the normal range. Since the decimation filter has the slowest time constant in the signal chain, the decimation filter sets the artifact recovery time. Fig. 4(c) illustrates the timing waveforms demonstrating the described problem and solution. A conventional phase quantizer becomes unstable when overloaded, leading to oscillations until the power is reset. The proposed phase quantizer detects saturation when the artifact is present and recovers quickly, minimizing data loss.

C. Bandwidth Scaling

Neural signals are categorized by their frequency band and require a power-scalable AFE based on the operation mode. The different modes provide flexibility for recording broadband or selecting bands of cortical neuronal activity. One way to scale down CT-$\Delta\Sigma$Ms integration bandwidth is by keeping the ADC clock rate constant and increasing the decimation factor. This improves signal-to-noise ratio (SNR) by 3 dB for every 2× reduction while maintaining the same power. Considering scenarios where hundreds of readout channels operate simultaneously inside the skull, efficient power scaling is important to enable operation with more channels at lower sampling rates while adhering to human tissue thermal limits.

Fig. 3 shows four operation modes supported by this design along with their bandwidth and loop coefficients: modes 0, 1, and 2 provide the capability of recording delta (1–4 Hz), theta (4–8 Hz), alpha (8–12 Hz), beta (12–40 Hz), gamma (40–100 Hz), and high-frequency oscillations (100–500 Hz), and mode 3 allows recording single unit and multiunit neuronal activity (500–10 000 Hz). Mode 0 satisfies requirements for clinical monitoring of activity below 500 Hz, and modes 1 and 2 allow oversampling of such activity. Mode 3 can be used for clinical monitoring and research to identify fast neuronal events that can be otherwise missed [47]. The CT-$\Delta\Sigma$M architecture mandates scaling integrator coefficients in line with f_{s} to maintain consistent loop dynamics. For the first integrator, we implement transconductance-based scaling, ensuring power scales proportionally with f_{s}. For the second integrator, CCO-based scaling is used to scale f_{CCO} and the quantizer power proportionally.

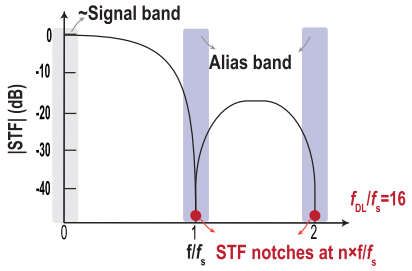


Fig. 5. Datalink noise immunity.

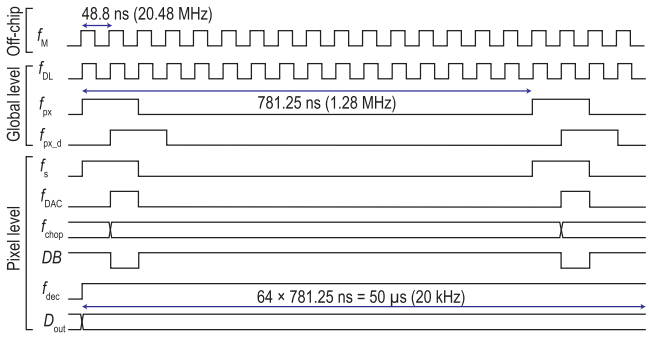


Fig. 6. On-chip timing signal generation (BW = 10 kHz).

D. System-Level Considerations

Several system-level decisions were made to ensure scalability to the future target of 1024 channels/pixels on a single chip. First, the decimation filter is implemented within each pixel, substantially reducing the datalink speed and power consumption, which is proportional to the OSR. Without the decimation filter, the required data link speed would reach 1.3 Gb/s for 1024 channels running at a 10 kHz BW, making wireless data transfer from a subcutaneous circuit impractical. This design also offers stronger antialiasing rejection of out-of-band signals compared to the PGA + multiplexed Nyquist ADC architecture since they typically use first- or second-order antialiasing filters with −6 or −12 dB/oct attenuation. Finally, for improved noise immunity, the serial data clock frequency, f_{DL}, is an integer multiple of f_{s} (across all modes). For shielding the ADCs from datalink noise, the energy is positioned in a null of the modulator's STF, as shown in Fig. 5.

For simplifying routing and to save power, each pixel generates its own intermediate timing signals for the ADC, as shown in Fig. 6. The chip receives an off-chip master clock, f_{M}, at 20.48 MHz (the same as f_{DL} for BW = 10 kHz, which is highest clock frequency on chip) to generate all on-chip timing signals. Two clock signals, f_{px} and $f_{\mathrm{px\_d}}$, run at the $\Delta\Sigma$ modulator's clock modulator frequency, with the latter delayed by 6.25% of T_{s}. These signals are generated at the global level and routed to the pixel array for further signal generation. The duty cycle of these signals was chosen to simplify the generation of the timing edges needed within the modulator. Edge timing based on inverter delays was avoided to minimize variation.

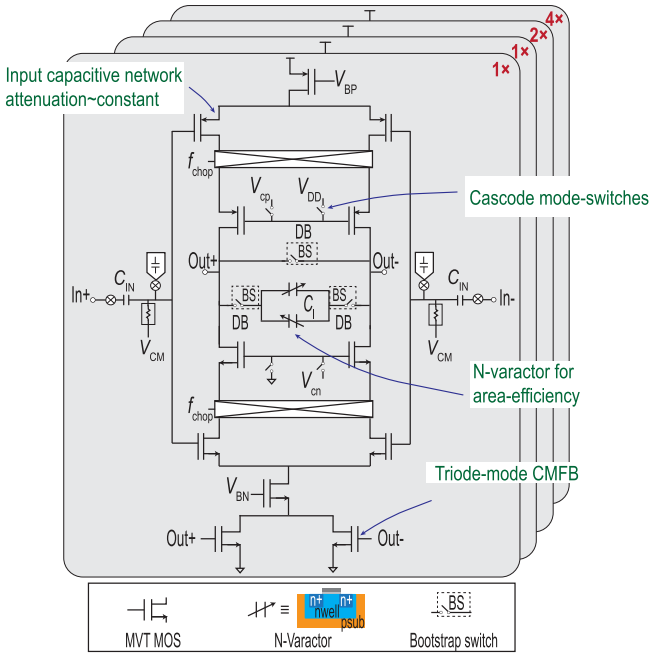


Fig. 7. Schematic of the G_m-C integrator.

IV. Circuit Implementation

A. G_m-C Integrator

Fig. 7 shows the implementation of the G_m-C integrator with the input chopper switches and ac-coupling capacitors. The ADC input is chopped and capacitively coupled through two 650-fF metal–insulator–metal (MIM) capacitors, C_{IN}, onto the PVG, a high-impedance node such that the input capacitive attenuation is 0.87. C_{IN} was selected to optimize the balance between the ADC's input impedance, C_{DAC} area, and the unit C_{DAC} element layout and mismatch constraints. The input chopper switches are clock boosted to $2V_{DD}$ to reduce the switches' ON-resistance and improve linearity without increasing their size. The input common-mode voltage, V_{CM}, is set through a pseudoresistor divider.

The G_m-C integrator incorporates transconductance-based coefficient scaling, comprising four parallel G_m branches with drive strength ratios 1:1:2:4, which are turned on/off through the cascode bias nodes. The G_m is scaled down by the same factor as f_s, keeping the integrator gain, G_m/f_sC_I, consistent. This topology ensures a nearly constant input capacitance from the 1st integrator, which helps keep the SNR constant due to input capacitive network attenuation across modes. It also has 2–8× more power and is more area efficient than scaling the integration capacitor C_I, and scaling the bias current alone is inaccurate.

Each branch comprises a dual-tail, complementary-input transconductor with a cascoded load. As the first block in the signal chain, optimizing this design for noise efficiency is critical for overall resolution. We, therefore, use complementary inputs to boost the noise efficiency by 2×, with both PMOS and NMOS inputs biased in sub-subthreshold for an effective G_m/I_D of 40 S/A. With a 3.2 fF unit C_{DAC} element, the input devices are near minimum size to preserve SNR against input capacitive network attenuation. The G_m is calculated by allocating 80% of the overall noise budget to its thermal noise. Medium V_t (MVT) devices were used to reduce the supply to 0.9 V and improve power efficiency. The differential input range of the first integrator is restricted to 15 mV_{pp} to minimize SQNR degradation due to quantization noise folding. The downmodulation chopper switches were implemented with small switches to reduce the gate capacitance, minimizing clock feedthrough and charge injection errors. Chopping lowers the flicker noise corner frequency from 32 kHz to <50 Hz, reducing its contribution from the dominant noise source to 5% of the 1st integrator's total noise. Cascode transistors reduce the integrator leakage (60 dB dc gain) and enable downmodulation at a low-impedance node for faster settling. The cascode transistors and current mirrors are biased in moderate inversion, meeting the target specifications (differential output swing of 100 mV_p) with 3σ yield. A triode-based common-mode feedback (CMFB) topology was used for its high input-linear range and stability. It senses the output common-mode voltage and adjusts the NMOS bias current via MOS resistors.

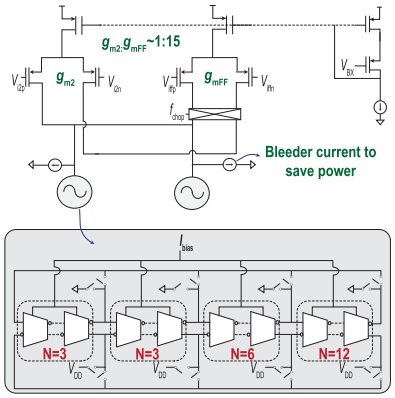


Fig. 8. Schematic of the time-based integrator.

In area-constrained designs, the size of the output capacitors in G_m-C filters is often a concern. To minimize area, C_I is implemented with NMOS varactors. The high capacitor density and differential topology save 4× area over MIM or metal–oxide–metal (MOM) capacitors. Connecting them in an antiparallel configuration also cancels their even-order nonlinearity. MOS capacitors are unsuitable for this topology since they must be biased in inversion or accumulation, restricting their use to single-ended use cases.

B. Time-Based Second Integrator

The second integrator comprises a ring-oscillator-based CCO that combines the G_m-cells of the direct (G_{m2}) and feedforward paths (G_{mFF}), as shown in Fig. 8. The CCO uses a pseudo-differential NMOS cross-coupled inverter architecture for noise efficiency [48]. First-order noise shaping provided by the loop relaxes the noise specifications of both G_m-cells and the CCO. G_{m2} and G_{mFF} maintain a 1:15 ratio, using unit devices with similar G_m/I_D as the G_m-C filter to ensure tracking of PVT variation. The gain of the second integrator is scaled across modes by changing the number of CCO stages with the same CCO bias current. This keeps the same rate of edges in the ring while scaling down the rate sent to the

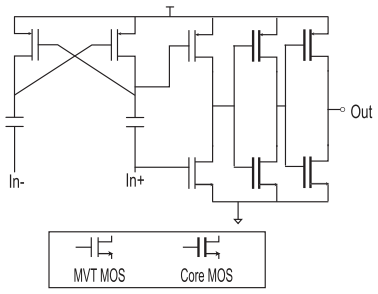


Fig. 9. Circuit implementation of the level shifter.

Gray counter. This method consumes 2–8× lower power than frequency divider-based scaling, where a divider would be after the level shifter. CCO-based scaling scales down f_{CCO} and the CCO gain, K_{ICCO}, by the same factor as f_s, keeping the integrator gain, K_{ICCO}/f_s, constant. Part of the current is bled off to reduce f_{CCO} to 10 MHz (typical), reducing the counter's power by 2×, which is important as f_{CCO} is 10 × f_s.

The level shifters following the CCO, which are required to drive the CMOS counters and phase quantizer, are implemented, as shown in Fig. 9. It uses a bootstrapped gate drive by decoupling the PMOS and NMOS driver with ac coupling [49]. Delay from level shifters is signal-dependent due to the variation in CCO output swing with the input signal, making delay reduction important. This topology reduces the large delay from contention between pull-down and pull-up transistors in a conventional latch in a power-efficient manner.

C. Quantizer and DAC

The CCO's phase is quantified using a counter-based quantizer. Since the CCO edges are asynchronous to the sampling instant, a Gray code counter avoids sampling errors by ensuring only one internal bit transitions at a time. The power of Gray counters is reduced by 40% compared to a binary counter with Gray-to-binary and binary-to-Gray encoders [43] by implementing a DFF-only counter, which directly counts in Gray code. This halves the power overhead of every additional bit, making the added power consumption of the circuitry that accommodates the two bits for overrange correction negligible. The ADC is passed through a first-order shaped tree-structured DEM encoder. The DAC unit elements are custom MOM capacitors for more flexibility during layout, with a 3.2-fF unit capacitance for a 4-bit thermometer-coded DAC. The ∼0.8% capacitor variation degrades the ADC's performance by less than 1 dB in simulation. Instead of re-clocking the DAC using DFFs, latches were used because they reduce errors caused in the event of quantizer metastability by allowing a "late" edge to propagate to the DAC immediately during the latch's transparent phase. All digital circuits used a custom design flow with a mix of standard cells and custom-designed circuits to optimize each block for power and area compared to standard logic synthesis and place-and-route flow.

D. Decimation Filter

The on-chip decimation filters decimate each ADC output by 64× to the Nyquist rate, using a third-order CIC filter

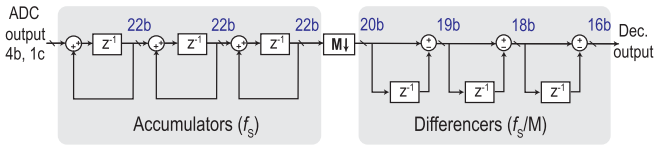


Fig. 10. Schematic of the decimation filter.

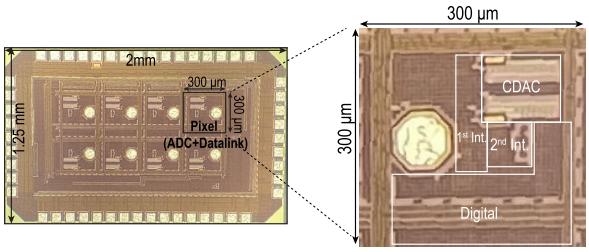


Fig. 11. Chip microphoto.

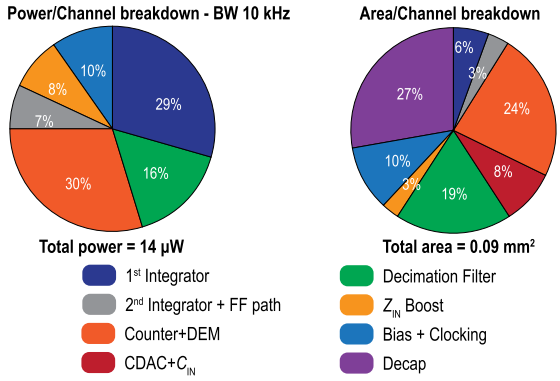


Fig. 12. Power and area breakdown.

with 16-bit output resolution, as shown in Fig. 10. This filter provides third-order antialias filtering for signals above $f_s/2$, exceeding typical filters in PGA-shared ADC architectures. The transfer function of the filter is

$$H(z) = \left[\frac{(1-z^{-64})}{(1-z^{-1})}\right]^3. \quad (1)$$

The register bit-widths of each stage were optimized using Hogenauer's register bit-pruning algorithm [50].

V. Measurement Results

This 8-pixel chip is fabricated in 180-nm CMOS, with each pixel occupying 0.09 mm^2. An annotated chip micrograph is shown in Fig. 11. An octagonal electrode pad, measuring 66 μm on metal layer 6, is added to facilitate the chip's interfacing with electrode grids through bumping, supporting a future expansion to 1024 pixels on a single chip with minimal design modifications. Each pixel consumes 14 μW from 0.9 and 0.7 V supplies for analog (53%) and digital (47%), respectively, as shown in Fig. 12. Section V-A describes the electrical measurements followed in vivo biological measurements in Section V-B.

A. Electrical Characterization

The chip was tested using an Audio Precision APx555B ultralow distortion signal source applying a 125-mV$_{pp}$

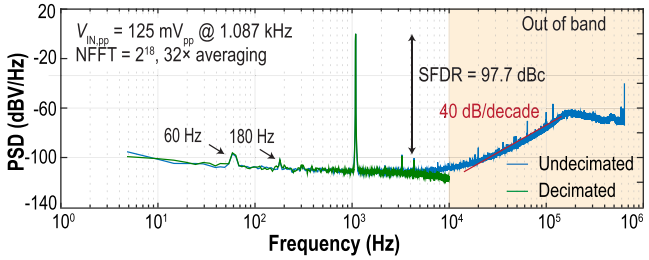


Fig. 13. Measured ADC output spectrum before and after in-pixel decimation filter.

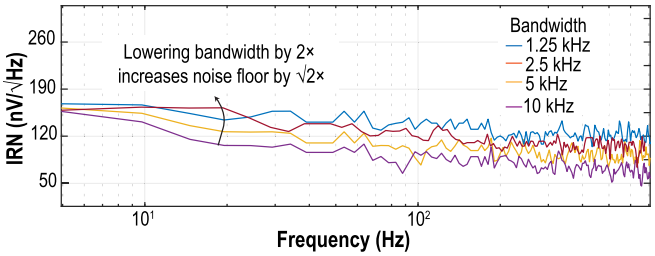


Fig. 14. Measured ADC IRN spectrum across modes.

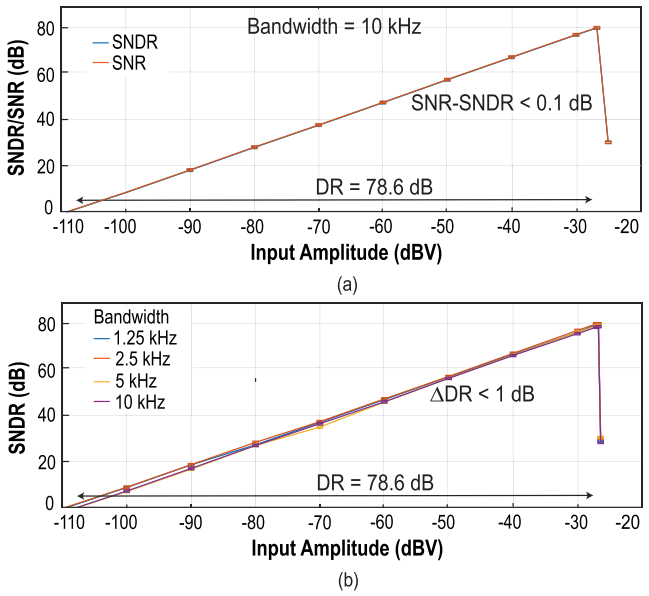


Fig. 15. (a) Measured SNR and SNDR for mode with BW = 10 kHz. (b) Measured SNDR across modes.

full-scale (FS) sinusoidal input at 1.087 kHz. Fig. 13 shows a measured spectrum with and without decimation filtering where the ADC achieves a 78.6 dB SNDR and DR in a 10 kHz bandwidth and an SFDR of 97.7 dBc with $f_s = 1.28$ MHz and an $f_s/2$ chopping clock. The 60- and 180-Hz tones are caused by power line interference. The characteristic 40 dB/decade noise shaping from a second-order modulator is apparent in the spectrum. The magnitude droop in the decimated output is typical of the sinc^3 function, which can be corrected in the ECoG system software using a simple filter

$$y[n] = 1.5x[n] - 0.5y[n-1]. \quad (2)$$

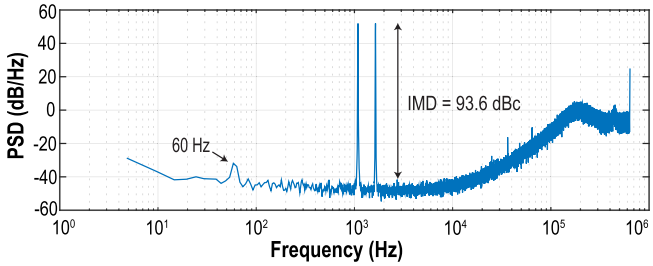


Fig. 16. Measured IMD.

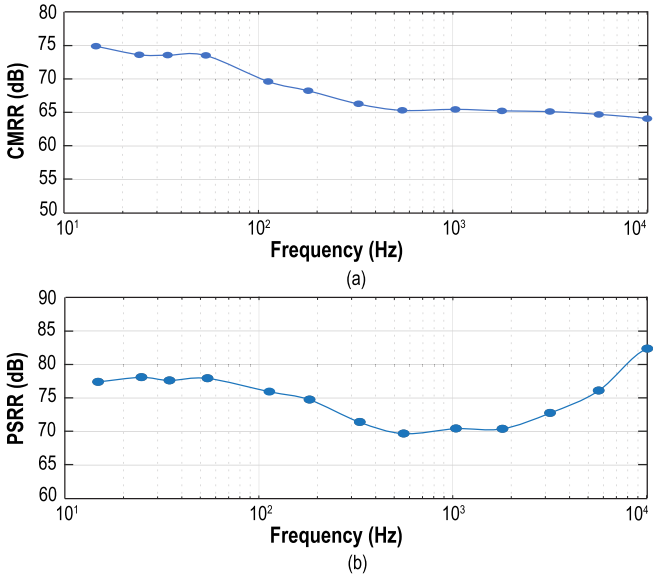


Fig. 17. Measured ADC (a) CMRR and (b) PSRR.

Typically, compensation FIR filters are used to correct for the magnitude droop of the CIC filters. The ADC IRN was measured with shorted inputs, and the corresponding power spectral density (PSD) is shown in Fig. 14. Because of the scalable architecture, the integrated IRN is constant (6 μV_{rms}) across the different modes. The DR was characterized by sweeping the input amplitude, achieving a 78.6 dB DR, as shown in Fig. 15, where the SNR and SNDR differ by $<$0.1 dB for the 10 kHz bandwidth mode. The DR across modes [Fig. 15(b)] differs by $<$1 dB as the FS range and IRN remains constant across modes.

Linearity is not a stringent requirement in this application due to the inherent nonlinearity of the electrodes. For completeness, this ADC was, however, tested for linearity by exciting it with two tones at -6 dBFS. Fig. 16 shows the measured intermodulation distortion (IMD) is 93.6 dBc. The CMRR was measured by applying a 10-mV$_{pp}$ signal to shorted inputs. The CMRR remains above 65 dB from dc to 10 kHz ($n = 5$, average $\sigma = 7$ dB), as shown in Fig. 17(a). The same process was repeated, with the signal applied to the analog supply voltage, VDD$_A$, to measure the power supply rejection ratio (PSRR). Fig. 17(b) demonstrates robustness against supply voltage variation, with better than 70 dB PSRR ($n = 5$, average $\sigma = 6$ dB). For completeness, the PSRR of the digital supply, VDD$_D$, was also measured at $>$100 dB.

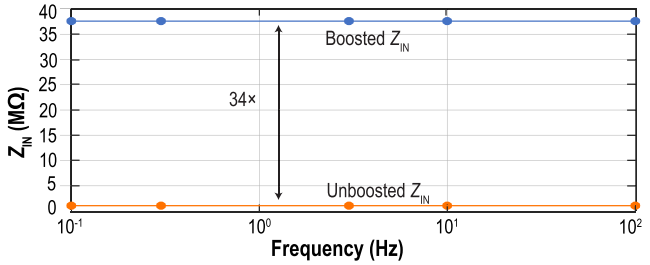


Fig. 18. Measured Z_{IN} with and without boosting.

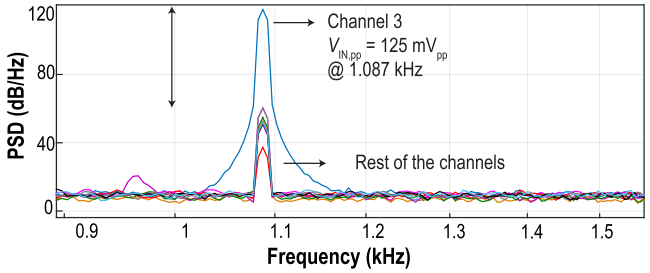


Fig. 19. Measured pixel-to-pixel isolation.

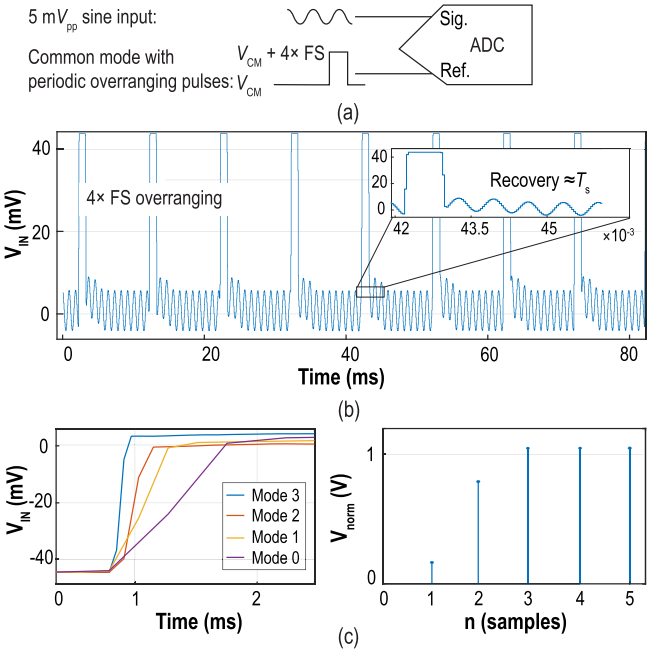


Fig. 20. Artifact recovery time (a) setup, (b) measurement in mode 3, and (c) measurement in all modes.

To measure the input impedance, Z_{IN}, high precision 1 MΩ resistors were placed in series with the ADC inputs, and an IA amplified the voltage across them. Fig. 18 shows Z_{IN} measured across the bandwidth with and without activating the auxiliary path, where Z_{IN} is boosted by 34× when the auxiliary path is enabled. Pixel-to-pixel isolation was measured by injecting an FS input into pixel 3 while shorting the inputs of the others. Fig. 19 plots the output spectrum of all pixels. The design has >60 dBc isolation for adjacent pixels with respect to the aggressor.

Finally, the artifact recovery time was measured using a function generator, as shown in Fig. 20(a), where the positive

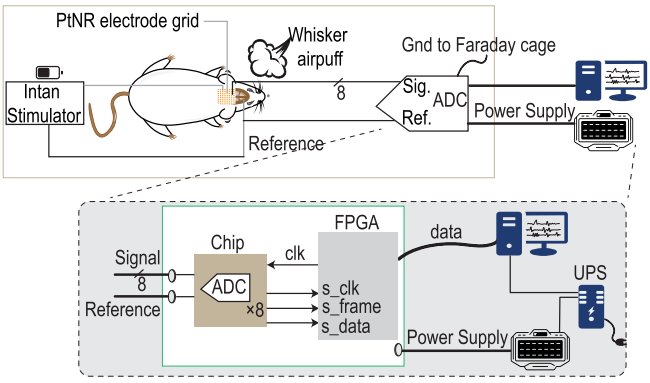


Fig. 21. In vivo measurement setup.

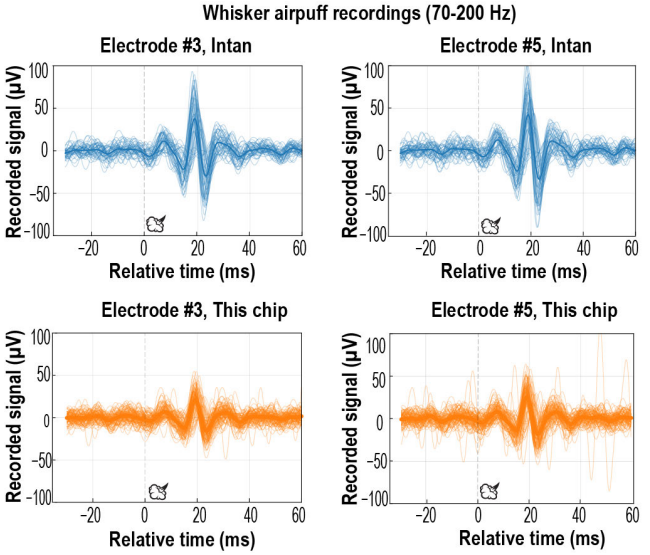


Fig. 22. Measured neural recordings with this chip and a commercial Intan chip.

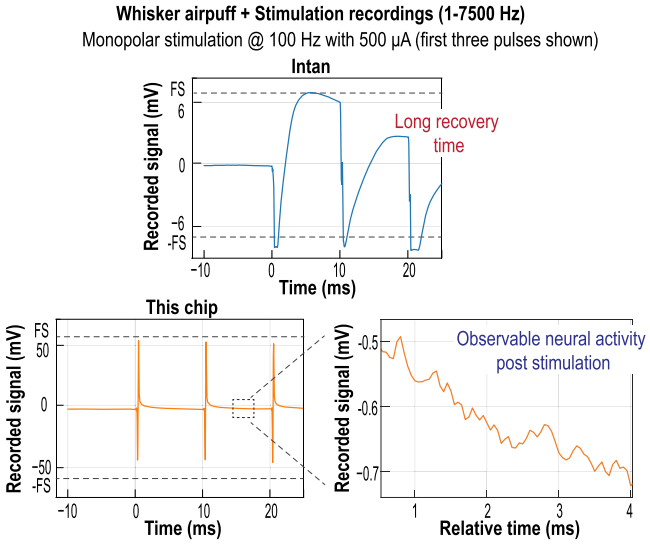


Fig. 23. Measured stimulation artifact recovery time for this chip and commercial Intan chip.

input was given a 5 mV_{pp} input, and the negative input was set at 450 mV with periodic overranging pulses of 4 × FS, varying between 450 and 950 mV. This drives the input to VDD_A,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO THE STATE-OF-THE-ART

Parameter	[19]	[30]	[23]	[26]	[38]	[34]	[36]	[32]	This work	
Topology	PGA + shared ADC				CT-ΔΣM					
Technology (nm)	500	130	65	65	110	180	180	22	**180**	
Supply (A/D) [V]	3.3	1.8/1.2	2.5	0.4-2.5	1	-	1.8	0.8	**0.9/0.7**	
# Pixels	64	384	1024	64	4	4	8	128	**8**	
Area/pixel (μm^2)	-	-	0.006	0.02	0.04	0.225	0.0046[d]	0.0045[d]	**0.073/0.09**[d]	
Input FS (mV_{pp})	10	10	4.87	50	300	200	15.2	21.5	**125**	
Bandwidth (kHz)	20	10	10	2.5	10	0.2	10	10	**1.25**	**10**
Power/pixel (µW)	830	49	2.72	5.2	8.6	3.9	-	5.57	**3.2**	**11.7**
Power/pixel with decimator (µW)	-	-	-	-	-	-	8.57	6.02	**3.5**	**14**
FoM_{SNDR} (dB)[c]	137	-	-	171	173	158	-	145	**163**[a]	**167**[a]
FoM_{SNDR} (dB)[c] **with decimator**	-	-	-	-	-	-	147	144.5	**162**[a]	**166**[a]
SFDR (dB)	-	-	-	-	94.2	91.2	63	59.49	**97**	**97.7**
EDO Tolerance (mV)	-	-	-	-	±150[e]	±100[e]	±60	Rail-to-rail	**±62.5**[e]	
IRN (μV_{rms})	2.4	6.36	8.98	2.2	6.6	1.3	4.46	7.71	**5.9**[a]	**6**[a]
Z_{IN} at DC (MΩ)	∞	∞	∞	>10[3]	∞	160	∞	∞	**304**	**38**
CMRR (dB)	82	>60	92	69	77	80	-	-	**75**	
Crosstalk (dBc)	-	64	>60	-	-	-	72	-	**>60**	
Stim. Artifact Tolerance	No			Yes	Yes		No		**Yes**	
Recovery Time (ms)	>> 100				-[b]	-[b]	-	-	**0.4**	**0.05**

[a] Averaged over 12 chips [b]Unusable beyond input range [c]Schreier FoM [dB] = SNDR + $10\log_{10}$(BW/Power) [d]With decimator
[e]EDO Tolerance = Input FS – neural signal

although the recovery time is not dependent on the input to the ADC, as the saturation detector of the quantizer works independently. The decimated output is plotted where the y-axis is input-referred [Fig. 20(b)]. The output saturates in the presence of the overranging pulse to 62.5 mV, the single-sided FS range of the ADC. The recovery time, defined as the period required to recover from saturation and resume recording, is dictated by the frequency response of the decimation filter (T_{dec}), as expected from the design. The ADC output recovers in one decimated sample (50 μs for 10 kHz BW). Fig. 20(c) shows the recovery time across modes and the step response of the decimation filter.

B. In Vivo Measurements

An in vivo brain recording experiment was performed to compare the performance with and without stimulation against a commercial chip, the Intan RHD2164 [19]. The electrode grid was composed of 8 platinum nanorod (PtNR) contacts [51] with 200 μm diameter and was placed on the primary somatosensory cortex of a rat. Mechanical deflections of the rat whiskers by timed and controlled air puffs lead to somatosensory evoked potentials measured by the electrodes. The precise topographic arrangement of the responsive regions is referred to as the whisker barrel cortex that our team used in prior studies to validate different electrode materials and recording systems [21], [52], [53]. Fig. 21 shows the measurement setup for the experiment conducted on a Sprague-Dawley rat implanted with PtNR electrodes. The electrode contact exhibited an impedance of ∼10 kΩ at 1 kHz in vivo. The impedance is predominantly capacitive at low frequencies, necessitating a high-impedance ADC to prevent signal attenuation. For evoking sensory activity, air puffs were delivered through a microcapillary tube using a PV830 pneumatic PicoPump (World Precision Instruments, Inc.) with 1-s pulses to individually stimulate the contralateral-side whiskers. Eight electrodes from the array were connected to eight recording pixels on either this chip or the Intan recording IC. A Pt wire inserted into the rat's skull was used as the reference electrode. The entire setup, including the rat and the recording front end, was placed in a Faraday cage connected to the ADC ground to filter out power supply interference according to animal protocol #S16020, approved by the Institutional Animal Care and Use Committee (IACUC) at the University of California, San Diego. The PC and measurement instruments were outside the cage. An FPGA (Opal Kelly XEM6310) provided the ADC clock, captured the data, and sent it to a PC for processing.

Fig. 22 compares somatosensory evoked potentials induced by 1 Hz air puffs on the rat's whiskers, recorded using the Intan system and this chip. ECoG activity (70–200 Hz) in response to the air puff was simultaneously captured across all eight pixels. Two pixels from each chip are shown, demonstrating comparable SNR. An Intan stimulator (RHS 2116) [54] was added to the test setup to compare the response in the presence of stimulation artifacts. All 16 stimulator channels were connected to 16 different electrodes, separate from the recording electrodes. During monopolar stimulation (500 μA at 100 Hz), the Intan front end saturated, resulting in data loss, as shown in Fig. 23. We chose monopolar stimulation for its larger volumetric stimulation impact and lower stimulation currents than bi-phasic stimulation. 500 μA was selected to demonstrate the chip's fast settling time even under high-current conditions, as it is the maximum current at which the 200 μm diameter PtNR contact remains below the water electrolysis threshold [55]. Given that 50–500 Hz is standard in clinical settings, 100 Hz was selected. Since the

Intan uses a PGA + shared ADC architecture for recording, it has a much lower input range (5 mV_p) than this chip. Additionally, the input high-pass network on the Intan results in a longer recovery time after saturation. In contrast, this chip outperformed by recovering with immediate observation of neural activity.

C. Comparison to the State-of-the-Art

Table I compares the performance of this work with recently published state-of-the-art neural recording front ends. The table is categorized by readout topology: PGA + shared ADC [19], [23], [26], [30], which uses capacitive input, and CT$\Delta\Sigma$M, which uses capacitive with [33] or without chopping [32], or G_m-input [34], [36], [38]. This work achieves the fastest (sub-ms) stimulation artifact recovery time. The recovery time of this work is >250× faster than existing solutions. This is the first work to address the artifact-induced instability problem associated with CT-$\Delta\Sigma$Ms using time-based quantizers [31], [34], [41], [43], making them suitable for clinical use. The chip is competitive in other metrics, including power consumption, noise performance, and robustness to variations. It supports multiple bandwidths with consistent performance and power scaling, allowing customization of the AFE for specific neural recording frequency bands.

VI. Conclusion

This article presents a 4 × 2 array of per-pixel 2nd-order CT-$\Delta\Sigma$Ms with a time-based ring-oscillator quantizer for direct digitization of neural recording signals in a closed-loop neuromodulation system. Each design decision was made to ensure the system is energy-efficient, robust, and scalable to the future target of 1024 pixels on a single chip. It achieves sub-ms artifact recovery time, enabling in-stimulation recording by preventing modulator instability, which is accomplished through fast recovery and overrange detecting phase quantizer. The ADC features a pseudo-virtual ground feedforwarding technique and a complementary input G_m-C filter with a per-pixel decimator, ensuring an efficient and optimized design. It supports four modes of recording 2.5–20 kS/s via a power-efficient, bandwidth-scalable CT-$\Delta\Sigma$M. The chip's performance was successfully validated through an in vivo whisker barrel rat experiment and compared against a commercial Intan chip, showing better artifact recovery time. This work demonstrates that time-based modulators can effectively record clinical ECoG signals in closed-loop neuromodulation systems.

References

[1] N. G. Pozzi and I. U. Isaias, "Adaptive deep brain stimulation: Retuning Parkinson's disease," *Handbook Clin. Neurol.*, vol. 184, pp. 273–284, May 2022, doi: 10.1016/B978-0-12-819410-2.00015-1.

[2] Y. Ezzyat et al., "Closed-loop stimulation of temporal cortex rescues functional networks and improves memory," *Nature Commun.*, vol. 9, no. 1, p. 365, Feb. 2018, doi: 10.1038/s41467-017-02753-0.

[3] A. S. Widge et al., "Treating refractory mental illness with closed-loop brain stimulation: Progress towards a patient-specific transdiagnostic approach," *Experim. Neurol.*, vol. 287, pp. 461–472, Jan. 2017, doi: 10.1016/j.expneurol.2016.07.021.

[4] A. L. Benabid, S. Chabardes, J. Mitrofanis, and P. Pollak, "Deep brain stimulation of the subthalamic nucleus for the treatment of Parkinson's disease," *Lancet Neurol.*, vol. 8, no. 1, pp. 67–81, Jan. 2009.

[5] L. R. Hochberg et al., "Neuronal ensemble control of prosthetic devices by a human with tetraplegia," *Nature*, vol. 442, no. 7099, pp. 164–171, Jul. 2006, doi: 10.1038/nature04970.

[6] A. B. Schwartz, X. T. Cui, D. J. Weber, and D. W. Moran, "Brain-controlled interfaces: Movement restoration with neural prosthetics," *Neuron*, vol. 52, no. 1, pp. 205–220, Oct. 2006.

[7] H. Duffau, "Contribution of intraoperative electrical stimulations in surgery of low grade gliomas: A comparative study between two series without (1985–96) and with (1996–2003) functional mapping in the same institution," *J. Neurol., Neurosurgery Psychiatry*, vol. 76, no. 6, pp. 845–851, Jun. 2005, doi: 10.1136/jnnp.2004.048520.

[8] N. C. Swann et al., "Adaptive deep brain stimulation for Parkinson's disease using motor cortex sensing," *J. Neural Eng.*, vol. 15, no. 4, Aug. 2018, Art. no. 046006, doi: 10.1088/1741-2552/aabc9b.

[9] M. Zhang, Z. Tang, X. Liu, and J. Van der Spiegel, "Electronic neural interfaces," *Nat. Electron*, vol. 3, no. 4, pp. 191–200, Apr. 2020.

[10] J.-J. Sit and R. Sarpeshkar, "A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6 nA DC error for 1-mA full-scale stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 172–183, Sep. 2007, doi: 10.1109/TBCAS.2007.911631.

[11] R. Vatsyayan et al., "Electrochemical and electrophysiological considerations for clinical high channel count neural interfaces," *MRS Bull.*, vol. 48, no. 5, pp. 531–546, May 2023, doi: 10.1557/s43577-023-00537-0.

[12] J. Yoo, L. Yan, D. El-Damak, M. A. B. Altaf, A. H. Shoeb, and A. P. Chandrakasan, "An 8-channel scalable EEG acquisition SoC with patient-specific seizure classification and recording processor," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 214–228, Jan. 2013.

[13] A. Chua, M. I. Jordan, and R. Müller, "SOUL: An energy-efficient unsupervised online learning seizure detection classifier," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2532–2544, Aug. 2022, doi: 10.1109/JSSC.2022.3172231.

[14] N. Butz, A. Taschwer, S. Nessler, Y. Manoli, and M. Kuhl, "A 22 v compliant 56 μW twin-track active charge balancing enabling 100% charge compensation even in monophasic and 36% amplitude correction in biphasic neural stimulators," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2298–2310, Aug. 2018, doi: 10.1109/JSSC.2018.2828823.

[15] H. Chandrakumar and D. Markovic, "An 80-mVpp linear-input range, 1.6-GΩ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mVpp common-mode interference," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, Nov. 2017, doi: 10.1109/JSSC.2017.2753824.

[16] S. Culaclii, B. Kim, Y.-K. Lo, L. Li, and W. Liu, "Online artifact cancelation in same-electrode neural stimulation and recording using a combined hardware and software architecture," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 3, pp. 601–613, Jun. 2018.

[17] A. Zhou, B. C. Johnson, and R. Müller, "Toward true closed-loop neuromodulation: Artifact-free recording during stimulation," *Current Opinion Neurobiol.*, vol. 50, pp. 119–127, Jun. 2018.

[18] D. A. Wagenaar and S. M. Potter, "Real-time multi-channel stimulus artifact suppression by local curve fitting," *J. Neurosci. Methods*, vol. 120, no. 2, pp. 113–120, Oct. 2002, doi: 10.1016/s0165-0270(02)00149-8.

[19] *Digital Electrophysiology Interface Chip*. Accessed: Jun. 26, 2024. [Online]. Available: https://intantech.com/files/Intan_RHD2164_datasheet.pdf

[20] A. Jain et al., "A 2.5–20kSps in-pixel direct digitization front-end for ECoG with in-stimulation recording," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*. CO, USA: IEEE, Apr. 2024, pp. 1–2, doi: 10.1109/cicc60959.2024.10529096.

[21] Y. Tchoe et al., "Human brain mapping with multithousand-channel PtNRGrids resolves spatiotemporal dynamics," *Sci. Translational Med.*, vol. 14, no. 628, Jan. 2022, Art. no. eabj1441, doi: 10.1126/scitranslmed.abj1441.

[22] R. R. Harrison and C. Charles, "A low-power low-noise CMOS for amplifier neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003, doi: 10.1109/JSSC.2003.811979.

[23] D. Yoon, S. Pinto, S. Chung, P. Merolla, T. Koh, and D. Seo, "A 1024-channel simultaneous recording neural SoC with stimulation and real-time spike detection," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.

[24] C. M. Lopez et al., "22.7 A 966-electrode neural probe with 384 configurable channels in 0.13μm SOI CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Jan. 2016, pp. 392–393, doi: 10.1109/ISSCC.2016.7418072.

[25] D. Han, Y. Zheng, R. Rajkumar, G. Dawe, and M. Je, "A 0.45V 100-channel neural-recording IC with sub-μW/channel consumption in 0.18μm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 290–291, doi: 10.1109/ISSCC.2013.6487739.

[26] J. Xu et al., "Fascicle-selective ultrasound-powered bidirectional wireless peripheral nerve interface IC," *IEEE Trans. Biomed. Circuits Syst.*, vol. 17, no. 6, pp. 1237–1256, Dec. 2023, doi: 10.1109/TBCAS.2023.3332258.

[27] R. Müller, S. Gambini, and J. M. Rabaey, "A 0.013 mm^2 5μW DC-coupled neural signal acquisition IC with 0.5 V supply," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2011, pp. 302–304, doi: 10.1109/ISSCC.2011.5746328.

[28] E. A. Brown, J. D. Ross, R. A. Blum, Y. Nam, B. C. Wheeler, and S. P. DeWeerth, "Stimulus-artifact elimination in a multi-electrode system," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 1, pp. 10–21, Mar. 2008, doi: 10.1109/TBCAS.2008.918285.

[29] N. S. K. Fathy, J. Huang, and P. P. Mercier, "A digitally assisted multiplexed neural recording system with dynamic electrode offset cancellation via an LMS interference-canceling filter," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 953–964, Mar. 2022.

[30] C. Mora Lopez et al., "A neural probe with up to 966 electrodes and up to 384 configurable channels in 0.13 μm SOI CMOS," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 3, pp. 510–522, Jun. 2017, doi: 10.1109/TBCAS.2016.2646901.

[31] C. Lee et al., "A 6.5-μW 10-kHz BW 80.4-dB SNDR G_m-C-Based CT $\Delta\Sigma$ modulator with a feedback-assisted gm linearization for artifact-tolerant neural recording," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2889–2901, Nov. 2020, doi: 10.1109/JSSC.2020.3018478.

[32] X. Yang et al., "An AC-coupled 1st-order Δ-$\Delta\Sigma$S readout IC for area-efficient neural signal acquisition," *IEEE J. Solid-State Circuits*, vol. 58, no. 4, pp. 949–960, Apr. 2023, doi: 10.1109/JSSC.2023.3234612.

[33] S. Wang et al., "A compact chopper stabilized Δ-$\Delta\Sigma$S neural readout IC with input impedance boosting," *IEEE Open J. Solid-State Circuits Soc.*, vol. 1, pp. 67–78, 2021, doi: 10.1109/OJSSCS.2021.3113887.

[34] H. Jeon, J.-S. Bang, Y. Jung, I. Choi, and M. Je, "A high DR, DC-coupled, time-based neural-recording IC with degeneration R-DAC for bidirectional neural interface," *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2658–2670, Oct. 2019.

[35] M. R. Pazhouhandeh, M. Chang, T. A. Valiante, and R. Genov, "Track-and-zoom neural analog-to-digital converter with blind stimulation artifact rejection," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1984–1997, Jul. 2020.

[36] D. Wendler et al., "A 0.0046-mm^2 two-step incremental delta-sigma analog-to-digital converter neuronal recording front end with 120-mvpp offset compensation," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 439–450, Feb. 2023, doi: 10.1109/JSSC.2022.3190446.

[37] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "Sub-μV_{rms}-noise sub-μW/channel ADC-direct neural recording with 200-mV/ms transient recovery through predictive digital autoranging," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3101–3110, Nov. 2018, doi: 10.1109/JSSC.2018.2870555.

[38] C. Lee et al., "A miniaturized wireless neural implant with body-coupled power delivery and data transmission," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3212–3227, Nov. 2022.

[39] H. Kassiri et al., "Rail-to-rail-input dual-radio 64-channel closed-loop neurostimulator," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2793–2810, Nov. 2017, doi: 10.1109/JSSC.2017.2749426.

[40] Y. Jung et al., "A wide-dynamic-range neural-recording IC with automatic-gain-controlled AFE and CT dynamic-zoom $\Delta\Sigma$S ADC for saturation-free closed-loop neural interfaces," *IEEE J. Solid-State Circuits*, vol. 57, no. 10, pp. 3071–3082, Oct. 2022, doi: 10.1109/JSSC.2022.3188626.

[41] C. Pochet, J. Huang, P. Mercier, and D. A. Hall, "A 174.7-dB FoM, 2nd-order VCO-based ExG-to-Digital front-end using a multi-phase Gated-Inverted-Ring oscillator quantizer," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 6, pp. 1283–1294, Dec. 2021, doi: 10.1109/TBCAS.2021.3133531.

[42] H. Chandrakumar and D. Markovic, "A 15.2-ENOB 5-kHz BW 4.5-μ W chopped CT $\Delta\Sigma$ -ADC for artifact-tolerant neural recording front ends," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3470–3483, Dec. 2018, doi: 10.1109/JSSC.2018.2876468.

[43] C. Pochet and D. A. Hall, "A pseudo-virtual ground feedforwarding technique enabling linearization and higher order noise shaping in VCO-based $\Delta\Sigma$ modulators," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3746–3756, Dec. 2022, doi: 10.1109/JSSC.2022.3202040.

[44] W. Jiang, V. Hokhikyan, H. Chandrakumar, V. Karkare, and D. Markovic, "A ±50-mV linear-input-range VCO-based neural-recording front-end with digital nonlinearity correction," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 173–184, Jan. 2017, doi: 10.1109/JSSC.2016.2624989.

[45] R. Theertham and S. Pavan, "Unified analysis, modeling, and simulation of chopping artifacts in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 2831–2842, Aug. 2019, doi: 10.1109/TCSI.2019.2907167.

[46] G. Taylor and I. Galton, "A reconfigurable mostly-digital delta-sigma ADC with a worst-case FOM of 160 dB," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 983–995, Apr. 2013, doi: 10.1109/JSSC.2013.2239113.

[47] A. C. Paulk et al., "Microscale physiological events on the human cortical surface," *Cerebral Cortex*, vol. 31, no. 8, pp. 3678–3700, Jul. 2021, doi: 10.1093/cercor/bhab040.

[48] W. Zhao et al., "A 0.025-mm^2 0.8-V 78.5-dB SNDR VCO-based sensor readout circuit in a hybrid PLL-$\Delta\Sigma$ m structure," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 666–679, Mar. 2020, doi: 10.1109/JSSC.2019.2959479.

[49] S. C. Tan and X. W. Sun, "Low power CMOS level shifters by bootstrapping technique," *Electron. Lett.*, vol. 38, no. 16, pp. 876–878, Aug. 2002, doi: 10.1049/el:20020627.

[50] E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. ASSP-29, no. 2, pp. 155–162, Apr. 1981, doi: 10.1109/TASSP.1981.1163535.

[51] M. Ganji et al., "Selective formation of porous pt nanorods for highly electrochemically efficient neural electrode interfaces," *Nano Lett.*, vol. 19, no. 9, pp. 6244–6254, Sep. 2019, doi: 10.1021/acs.nanolett.9b02296.

[52] Y. Tchoe et al., "An electroencephalogram microdisplay to visualize neuronal activity on the brain surface," *Sci. Translational Med.*, vol. 16, no. 744, Apr. 2024, Art. no. eadj7257, doi: 10.1126/scitranslmed.adj7257.

[53] Y. Tchoe et al., "Considerations and recent advances in nanoscale interfaces with neuronal and cardiac networks," *Appl. Phys. Rev.*, vol. 8, no. 4, Dec. 2021, Art. no. 041317, doi: 10.1063/5.0052666.

[54] *Digital Electrophysiology Stimulator/Amplifier Chip*. Accessed: May 29, 2024. [Online]. Available: https://intantech.com/files/Intan_RHS2116_datasheet.pdf

[55] R. Vatsyayan and S. A. Dayeh, "A universal model of electrochemical safety limits in vivo for electrophysiological stimulation," *Frontiers Neurosci.*, vol. 16, Oct. 2022, Art. no. 972252.

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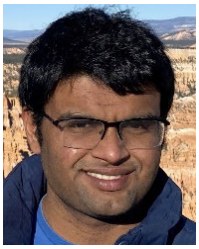

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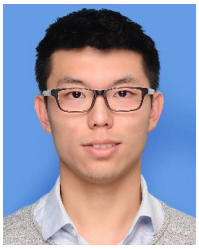

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