Influence of surface states on the extraction of transport parameters from InAs nanowire field effect transistors

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The capacitive effects of interface trap states in top-gated InAs nanowire field effect transistors and their influence on the experimental extraction of transport parameters are discussed. Time resolved transfer characteristics exhibit transient behavior indicating surface state trapping and detrapping with long characteristic time constants of 45 s. Varying gate voltage sweep rate results in a time-dependent extrinsic transconductance: a reduced gate voltage sweep rate leads to a charge neutral interface, reduced interface state capacitance, higher measured transconductance, and minimal hysteresis. These results demonstrate that measurements with a charge neutralized or passivated surface are key to extract intrinsic nanowire transport parameters.

Semiconductor nanowires (NWs) have attracted intense research interest due to their potential applications in electronic and photonic devices and integrated functional systems. As nanowires are of particular interest for potential high-speed nanoelectronic applications due to their high electron mobilities. However, the electronic and optoelectronic properties of NW devices are dramatically affected by surface and interface states due to their large surface area to volume ratio. While these effects can be desirable in some applications such as highly sensitive photodetectors, chemical and biological sensors, or may be detrimental for transport properties of nanowire field-effect transistors (NWFETs). Thus, understanding and quantifying the effects of surface states is necessary to accurately assess the intrinsic NW parameters and to enable control over and optimization of NW device performance.

In this letter, we present an investigation of the capacitive effects of surface states on the analysis of transport properties of InAs NWFETs, where (1) the transfer characteristics of the NWFETs are strongly dependent on gate voltage sweep rate; (2) the hysteresis in the transfer characteristics can be minimized and eliminated by reducing the gate voltage sweep rate, suggesting that slow sweep rates yield measurements that are most representative of the intrinsic nanowire carrier transport behavior; and (3) a circuit model analysis by including the effects of the interface states capacitance and the intrinsic transcondutance is developed to analyze the transport behavior.

InAs NWs for these studies, with diameters of 60–120 nm and lengths of ~10 µm, were grown by metal-organic chemical vapor deposition on a SiO2/Si substrate with V/III ratio of 50 at 350 °C and the top-gated NWFETs were fabricated on 600 nm SiO2/n+-Si utilizing e-beam lithography for Ti/Al source-drain contact leads and Al top gate patterning. A 73 nm rf sputtered ZrO2/Y2O3 layer extending over the source-drain contacts served as a gate dielectric. The Ti/Al contact resistance in a low Ohmic contact resistance of 1–10 kΩ due to surface Fermi energy pinning and electron accumulation at the InAs surface.

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in Fig. 1(c), accounts well for our experimental observations.

Figure 2 shows sweep-rate-dependent transfer characteristics obtained from an InAs NWFET at $V_{DS}=0.5$ V (the sweep direction is from negative to positive gate voltages). First, at the lowest sweep rates, $I_{DS}$ exhibits a decay at negative $V_{GS}$ in the off region prior to reaching $I_{off}$ (lowest $I_{DS}$ value). Once $V_{GS}$ is above the threshold voltage, the gate transconductance overcomes the $I_{DS}$ transient decay and the current increases. This unusual property in the transfer characteristics has not been discussed in the literature. These “tails” in $I_{DS}-V_{GS}$ in Fig. 2 can be attributed to changes in surface state charge that are apparent when the sampling time is comparable to or longer than the characteristic time constant of surface traps. Second, the slope of the transfer curves increases with reduced sweep rates. Slow sweep rates allow surface states to attain charge neutrality and thus minimize $C_{int}$, which results in higher transconductance values (1 $\mu$S for $10^3$ V/s and 12 $\mu$S for 1.7 mV/s). Correspondingly, the apparent $\mu_{FE}$ increases as the sweep rate is reduced. Table I summarizes the apparent mobility values obtained from Eq. (1) without considering the interface state effects, i.e., with $C_{int}/C_{acc}=0$. These results indicate that NW parameters extracted from FET characteristics may not represent the intrinsic values, but instead are highly dependent on measurement conditions. Measurements with low sweep rates (i.e., reduced $C_{int}$) are expected to yield transport parameters that are close to the intrinsic values of the InAs NWs. Moreover, the high field-effect mobility values confirm the potential of InAs NWs with proper surface passivation for high speed electronic applications.

The interface states also affect the estimate of mobile carrier concentration in the channel, which is given by $n_{channel}=I_{DS}L_{G}/\mu_{FE}V_{DS}A$, where $\mu_{FE}$ is obtained from Eq. (1). The total carrier concentration in the channel decreases as the $V_{GS}$ sweep rate is reduced, which is evident in the lower $I_{off}$ values at negative $V_{GS}$ as shown in Fig. 2. Also summarized in Table I are the computed carrier densities for this NWFET, measured with different $V_{GS}$ sweep rates. Note that the effect of interface state charge on $n_{channel}$ is different from those observed in GaN/AlGaN based heterojunction FETs, where the interface state charges in the gate-drain extension act as a surface virtual gate and cause further depletion of the channel and $n_{channel}$ can be restored with proper passivation. In these NWFETs, the interface state charges reduce the gate field and depletion width in the partially depleted NW channel underneath the gate.

In order to quantify the characteristics of the interface states, we performed time resolved transient measurements of these InAs NWFETs plotted in Fig. 3, which clearly show transient characteristics we attribute to surface state trapping and detrapping. $V_{DS}=0.5$ V was applied across the NWFET, and the current $I_{DS}$ was monitored while $V_{GS}$ was switched every 150 s in the following sequence: 0, -4, 0, +4, 0, ..., -1, 0, +1, 0 V. Long characteristic time constants up to 45 s were obtained from stretched exponential fittings to $I_{DS}(t)$ decays.

Only transients for $V_{GS}<0$ are shown in Fig. 3 for clarity. Figure 4 shows $I_{DS}-V_{GS}$ measurements for the same device obtained with different sweep rates. The dashed lines show $I_{DS}$ when $V_{GS}$ is swept with a rate of 10 V/s, for which hysteresis is clearly observed, and the solid lines in

<table>
<thead>
<tr>
<th>$V_{GS}$ sweep rate (V/s)</th>
<th>Apparent carrier concentration $n$ (cm$^{-3}$)</th>
<th>Apparent carrier mobility $\mu_{FE}$ (cm$^2$/Vs)</th>
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<td>1000</td>
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<tr>
<td>0.001 67</td>
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</table>

FIG. 1. (Color online) (a) Schematic diagram of the top-gated InAs NWFET with its dc equivalent circuit. Top left inset is the equivalent capacitance circuit model for the InAs NWFET including the interface capacitance $C_{int}$. Top right inset is a representative field emission scanning electron microscope image of the top-gate InAs NWFET. (b) $E_c$ band-edge profile along the center of the NW channel with $V_{DS}=0.5$ V and $V_{GS}=-4$ V, including interface traps that can detraps electrons for long gate voltage hold time. (c) Charge density distribution upon negative applied $V_{GS}$ when interface states are charged, or charge neutral leading to wider depletion depths into the channel.

FIG. 2. (Color online) Transfer curves of an InAs NWFET with different $V_{GS}$ sweep rates.

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dicate transfer characteristics with a sweep rate of 6.7 mV/s, for which hysteresis is dramatically reduced. Besides the effect on hysteresis, there also exists a pronounced difference in the current level at negative $V_{GS}$ for measurements with different sweep rates. The current level for the slow sweep rate is lower than that with the faster sweep rate which agrees well with the charge balance model depicted in Fig. 1. For slower sweep rates, the interface states are quasineutral and the depletion width extends deeper into the channel. As a result, the leakage path under the gate is reduced and the off-state $I_{DS}$ drops.

Using the equivalent capacitance model shown in Fig. 1, one can also estimate the density of interface states ($\eta_{it}$ = $C_{int}/q$, where $q$ is the fundamental charge constant) from straightforward circuit analysis:

$$\frac{Q_{acc}}{A} = C_{acc} \Psi_s = \frac{C_{ox}}{1 + \frac{C_{int}}{C_{acc}} + \frac{C_{ox}}{C_{acc}} (V_{GS} - V_t)},$$

(2)

where $\Psi_s$ is the surface potential at the oxide-InAs interface, $A$ is the effective NW surface area under the gate, and $V_t$ is the threshold voltage. $C_{ox}/C_{acc}$ is negligible due to the large oxide thickness as compared to the small spatial separation between the accumulation charges and the interface. Note that any bulk traps contribute to a much smaller capacitance between the accumulation charges and the interface. The ratio of the transconductance of the NWFET with neutralized interface states $g_{m1}$ to that with surface charges $g_{m2}$ then obeys the relationship

$$1 + \frac{C_{int}}{C_{acc}} = g_{m1}/g_{m2}.$$  

(3)

Assuming that the interface states are neutral for the gate sweep with 6.7 mV/s in Fig. 4, $g_{m1}/g_{m2} = 35 \mu S/15 \mu S = 2.3$. If a ~10 nm separation between the accumulation layer and the InAs/oxide interface is assumed (from one-dimensional Schrödinger-Poisson solution), the interface state capacitance can be calculated from Eq. (3) to be ~2 $\mu F/cm^2$. This value corresponds to an interface state density of ~4 x $10^{12}$ $cm^{-2}$ by assuming the traps to be uniformly distributed over 0.34 eV ($\sim E_F$) for InAs, which agrees well with values used to fit experimental data in similar InAs NWFETs.

In summary, we have fabricated InAs NWFETs and investigated the capacitive effects of surface states on the FET transport properties. The InAs NWFETs exhibited transient behavior that severely affects characteristic NW parameter extraction. From circuit and device analyses, we obtain apparent field-effect mobility values in the range of 1000–16,000 $cm^2/V s$ and surface state density in the low $10^{12} cm^{-2}$ range. The upper end of the mobility range is believed to best reflect the values intrinsic to transport within the NW. This analysis may help explain the wide range of NW parameters reported in the literature, which indicates that measurements with a charge neutralized (or passivated) surface allow the extraction of the intrinsic nanowire transport parameters, and highlights the potential of InAs NWs for high speed electronics with effective surface passivation.

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