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Strong room-temperature negative transconductance in an axial Si/Ge hetero-nanowire tunneling field-effect transistor

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We report on room-temperature negative transconductance (NTC) in axial Si/Ge hetero-nanowire tunneling field-effect transistors. The NTC produces a current peak-to-valley ratio $\gg45$, a high value for a Si-based device. We characterize the NTC over a range of gate $V_G$ and drain $V_D$ voltages, finding that NTC persists down to $V_D = -50$ mV. The physical mechanism responsible for the NTC is the $V_G$-induced depletion in the $p$-Ge section that eventually reduces the maximum electric field that triggers the tunneling $I_D$, as confirmed via three-dimensional (3D) technology computer-aided design simulations. © 2014 AIP Publishing LLC [http://dx.doi.org/10.1063/1.4892950]

Since the pioneering work of Esaki on the negative differential resistance (NDR) in highly doped $p$-$n$ junctions due to interband tunneling of carriers through a narrow potential barrier,1 NDR and negative transconductance (NTC) devices based on quantum mechanical tunneling have been heavily investigated because of their potential applications in low-power inverter logic, memory, and high-speed switching circuits.2-7 However, most of the early results were based on III-V semiconductors and suffered from the relatively low peak-to-valley ratio (PVR) at room temperature. Since then, many efforts were made to improve the device performance in silicon technology-compatible materials, including Si8 and Si/SiGe9 diodes based on forward-biased interband tunneling with improved PVR ($\sim5$), Si-based field-effect transistors,10-12 as well as new materials such as Ge-on-insulator,13,14 and Ge$_{x}$Si$_{1-x}$ metal-oxide-semiconductor field-effect transistors.15 Recently, semiconductor nanowires (NWs) have received much attention, and room-temperature NDR was reported in InP,16 Si,17 and Si/SiGe NWs.18 Silicon-based NTC devices operating at room temperature with high PVR would have the added advantage of plausible compatibility with modern silicon technology.

Here, we report on NTC in an axial Si/Ge hetero-NW tunneling field-effect transistor (TFET) structure with PVR $\gg45$, a high value for room-temperature operation in any material, but especially in Si. The NTC persists over a large range of drain voltage $V_D$ down to 50 mV and a reasonably low gate voltage $V_G < 1.5$ V. The NTC is repeatable, reproducible from device to device, and is observed in both up and down $V_G$ sweep directions, with some hysteresis due to charge trapping at the insulator/semiconductor interface, as verified by technology computer-aided design (TCAD) simulations.

The axial $n$-Si/$i$-Si/p-Ge hetero-NWs were grown on Ge (111) substrate by an Au-catalyzed vapor-liquid-solid (VLS) chemical vapor deposition method.19,20 The growth details can be found in a previous publication.21 The $p$-$i$-$n$ NW segments were $\sim2.5$ $\mu$m $p$-Ge, $\sim1.6$ $\mu$m $i$-Si, and $\sim3.4$ $\mu$m $n$-Si, with a diameter of $\sim55$ nm. The heterojunction transition between the Ge and Si section is estimated to be $\sim20–50$ nm wide, comparable to the NW diameter.22 This relatively sharp interfacial transition from $100$% Ge to $100$% Si for axial NW growth was achieved by in-situ switching the VLS liquid growth catalyst from Au to AuGa at the start of Si NW growth.23 A large fraction of the hetero-NWs are kinked at the Ge/Si junction, which could be avoided by optimizing the growth conditions,20,22 but they were in fact preferentially chosen during the device fabrication process to help locate the junction for top-gate placement.

After the growth, the NWs were ultrasonically dispersed in isopropanol and spread on a heavily p-doped silicon substrate covered with $\sim100$ nm of thermally grown SiO$_2$. Contacts to $p$-Ge and $n$-Si, doped in the low to mid-$10^{18}$ $\text{cm}^{-3}$ range, were realized by e-beam lithography (EBL), followed by e-beam evaporation of $120$ nm Ni contact metal and lift-off. Thereafter, $\sim10$ nm of high-$\kappa$ HfO$_2$ was deposited at $200^\circ\text{C}$ by atomic layer deposition, simultaneously annealing the Ohmic contacts. The top gate electrode was fabricated by a second EBL step, $100$ nm Ni evaporation and lift-off. The gate was aligned to cover the intrinsic Si section and parts of the $n$-Si and $p$-Ge sections, as shown in the scanning electron microscope (SEM) image of the final top-gated device in Fig. 1(a). Note that compared to the previously reported TFETs fabricated from hetero-NWs grown in the same batch,21 here the overlap of the $p$-Ge section is larger, which, as discussed below, enables the high PVR of our NTC devices.

Figure 1(a) shows the $I_D-V_G$ transfer characteristics at a fixed reverse source-drain voltage $V_D = -0.2$ to $-0.8$ V in $0.2$ V steps (with $n$-Si source grounded), including the relatively sharp turn-on of the current at a threshold $V_T$ (with the
Excellent NTC was observed for different devices were measured and showed similar behavior. The gate leakage current $I_D < 5 \text{ pA}$ for all $V_G$. (b) TCAD simulation of the conduction and valence band diagram cut along the device length at $V_D = -0.6 \text{ V}$ and $V_G = 0.5 \text{ V}$ (the gate overlaps the $i$-Si region, as well as parts of $n$-Si source and $p$-Ge drain).

best subthreshold slope of $\sim 55 \text{ mV/decade}$ over $\sim 3$ orders of $I_D$ at $V_D = -0.2 \text{ V}$ followed by current peak at a $V_P$ in the $0 < V_G < 1 \text{ V}$ range, and a strong NTC for $V_G > V_P$. Both $V_I$ and $V_P$ depend on $V_D$, shifting to lower $V_G$ as $V_D$ becomes more negative. Figure 1(b) shows the simulated band diagram of the device at the center of the channel along the NW axis in the TFET mode, with reverse-bias $V_D = -0.6 \text{ V}$ and $V_G = 0.5 \text{ V}$, where the $i$-Si channel under the gate is flooded with electrons. The arrow indicates electron tunneling controlled by the maximum electric field $E_{MAX}$ that, for these bias values, occurs in the narrow-gap Ge drain.

The $I_D - V_G$ characteristics of our devices on a linear scale, with a constant reverse $V_D$ applied to the $p$-Ge contact while keeping $n$-Si source and Si substrate grounded and sweeping the top-gate voltage $V_G$ are shown in Fig. 2 (several devices were measured and showed similar behavior). Excellent NTC was observed for different $V_D$ with PVR ranging from 20 to $>45$, with the highest PVR of 47.9 observed at $V_D = -0.2 \text{ V}$. The peak current positions $V_P$ and magnitudes vary somewhat depending on whether $V_G$ is swept up from $V_G = -1 \text{ V}$ (below threshold voltage $V_T$) as in Fig. 2(a), or down from $V_G = 2.5 \text{ V}$ as in Fig. 2(b). The inset in Fig. 2(b) presents the hysteresis between the upward and downward $V_G$ sweeps at $V_D = -0.6 \text{ V}$. The magnitude of the hysteresis ranges from $\sim 0.2 \text{ V}$ at $V_D = -0.8 \text{ V}$ to $\sim 0.5 \text{ V}$ at $V_D = -0.2 \text{ V}$. We attribute the hysteresis behavior to the charge trapping and detrapping at the Si/HfO$_2$ and Ge/HfO$_2$ interfaces, consistent with the TCAD simulations discussed below. It is likely that the hysteresis could be reduced by post-deposition annealing at elevated temperature in N$_2$ ambient; conversely, such charge-trapping-induced hysteresis may have memory applications.

Turning to the physical mechanism responsible for the NTC, we emphasize that, unlike some reported NTC devices where the decrease in $I_D$ was due to current diverted to gate leakage, $I_G$, in our device $I_G < 5 \text{ pA}$ for all $V_G$. Therefore, the NTC behavior should be explained by the tunneling at the heterojunction. The physical mechanism responsible for the NTC behavior is as follows: in the $V_T < V_G < V_P$ gate bias range, tunneling current increases as a result of the decreasing of the tunnel-barrier width. However, when $V_G$ exceeds $V_P$, tunneling current drops because the gate voltage begins to deplete carriers in the $p$-Ge section resulting in lower $E_{MAX}$ at the tunneling heterojunction. Note that a weak NTC signature was observed in our previous hetero-NW TFET publication, but the effect is stronger when the overlap of the top gate over the $p$-Ge section is larger, as in our case here, which further supports the postulated NTC mechanism.

In order to verify our experimental result, 3D TCAD simulations were performed using Synopsys Sentaurus. A two-dimensional cross-section through the middle of the
device along the hetero-NW is shown in Fig. 3(a). The simulation set-up is similar to that described in Ref. 21, except that the overlap over the p-Ge section of the top gate contact is 20 nm longer, which will effectively deplete carriers in p-Ge section near the junction at high $V_G$. The doping of the p-Ge and n-Si was taken as $5 \times 10^{15}$ cm$^{-3}$. The decay of the doping into i-Si (assumed to be $10^{15}$ cm$^{-3}$ p-Si due to background doping) was taken as 6 nm per decade of doping and the SiGe transition section was assumed to occur linearly over 50 nm. Since the Ge/high-$\kappa$ surface is known to have a high trap density, which is a main cause of the threshold voltage instability, a positive interface charge density $N_T \approx 10^{13}$ cm$^{-2}$ was assumed to shift the threshold voltage $V_T$ to approximately our experimental value. Figures 3(b) and 3(c) show, respectively, the spatial distribution of electron band-to-band tunneling generation at the tunneling junction at $V_D = -0.6$ V with $V_G = 0$ V (below $V_F$) and $V_G = 1$ V (above $V_F$, in the NTC part of the characteristic, see Fig. 1(a)). As evident from the figure, electrons tunnel from valence band of the p-Ge drain to the conduction band of the i-Si channel and the predicted tunneling generation at $V_G = 0$ V (Fig. 3(b)) is larger than that of at $V_G = 1$ V (Fig. 3(c)). The edges of the depletion region, shown by the white line in both figures, indicate how the highly doped drain has been depleted by the electric field due to the higher gate bias at $V_G = 1$ V, resulting in lower $E_{MAX}$ at the tunneling heterojunction and thus decreasing $I_D$.

The resulting simulated $I_D - V_G$ curves at constant $V_D$ are shown in Fig. 4. As can be seen, the simulation results in Fig. 4(a) are in reasonable quantitative agreement with the measured results in Fig. 2, including a simulated current PVR in the 10–30 range. Reproducing the hysteresis in the NTC with respect to the V$_G$ sweep direction, a slightly higher $N_T = 1.5 \times 10^{13}$ cm$^{-2}$ was assumed for the downward $V_G$ sweep than the $N_T = 1.4 \times 10^{13}$ cm$^{-2}$ for the upward sweep, consistent with the additional charging of the interface by the high $I_D$ flowing through the TFET at $V_G = 2.5$ V. As shown in Fig. 4(b), the location of peak current shifted negatively and the current increases at higher $N_T$, in agreement with our experimental data in Fig. 2.

In summary, we have demonstrated strong room-temperature NTC in axial n-Si/i-/Si/p-Ge hetero-NW TFETs with HfO$_2$ gate dielectric. The highest PVR of 47.9 was observed at reverse bias voltage of $-0.2$ V. We explain it by the $V_G$-induced depletion in the p-Ge section that eventually reduces the maximum electric field, which was confirmed by a 3D Sentaurus TCAD simulation. The ability to achieve a high PVR in Si-based devices at room temperature may be a step towards the realization of its application in logic and memory circuits.

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FIG. 3. (a) A cross-section through the hetero-NW in the 3D Sentaurus TCAD model: an n-doped Si substrate (not shown), a 100 nm thick SiO$_2$, a straight cylindrical NW of 50 nm diameter, a 10 nm thick HfO$_2$ gate oxide, and nickel “omega” gate metal (not to scale). Vertical lines in the channel indicate the boundaries of the SiGe transition region between i-Si channel and p-Ge drain; (b) and (c) Spatial distribution of band-to-band tunneling generation at the drain side at $V_D = -0.6$ V with (b) $V_G = 0$ and (c) $V_G = 1$ V. The white line in (b) and (c) indicates the edge of the depletion region in the p-Ge drain. The color scale bar indicates the magnitude of the generation in cm$^{-3}$ s$^{-1}$. Note the higher predicted tunneling generation (red-colored regions) at $V_G = 0$ (b) than at $V_G = 1$ V (c).

23 Synopsis Sentaurus TCAD ver. H-2013.03 using nonlocal band-to-band tunneling model.