Intrinsically Linear Transistor for Millimeter-Wave Low Noise Amplifiers

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ABSTRACT: Transistors are the backbone of any electronic and telecommunication system but all known transistors are intrinsically nonlinear introducing signal distortion. Here, we demonstrate a novel transistor with the best linearity achieved to date, attained by sequential turn-on of multiple channels composed of a planar top-gate and several trigate Fin field-effect transistors (FETs), using AlGaN/GaN structures. A highly linearized transconductance plateau of >6 V resulted in a record linearity figure of merit OIP3/PDC of 15.9 dB at 5 GHz and a reduced third-order intermodulation power by 400 dBf/cm² per tone at 10 MHz. The proposed architecture also features an exceptional performance at 30 GHz with an OIP3/PDC of ≥8.2 dB and a minimum noise figure of 2.2 dB. The device demonstrated on a scalable Si substrate paves the way for GaN low noise amplifiers (LNAs) to be utilized in telecommunication systems, and is also translatable to other material systems.

KEYWORDS: Linear, GaN, mm-wave, low noise amplifier

A wide dynamic range is fundamental to the operation of any system, particularly for amplifiers in wireless communication systems. The output current of an amplifier is fundamentally related to the input voltage signal by a nonlinear transconductance, g_m, whose higher order terms lead to intermodulation products with frequencies close to that of the fundamental signal, thereby invading the bandwidth of the amplifier and draining its available power. Conventional transistors have a bell-shaped g_m curve as a function of V_G, that is attributed to several physical origins including (i) self-heating effects, (ii) increase of the dynamic source access resistance, (iii) emission of optical phonons, and (iv) contact barriers. Transistors with vertically stacked multiple quantum well channels were hypothesized to lower g_m nonlinearities, but these were not practically utilized. Innovative material approaches including the use of nitrogen-polar surfaces on gallium nitride (GaN) and source regrowth advanced the linearity figure of merit, the ratio of output third-order intermodulation intercept point (OIP3) to DC power (P_DC), OIP3/P_DC, to 13.3 dB. The limited transistor linearity is often addressed with circuit linearization techniques employing derivative superposition (DS) and cancellation that can extend transistor linearity at low frequencies but become difficult to implement at high frequencies and cannot handle signals with sufficiently large power.

Linear GaN FETs should be capable of resolving transconductance degradation due to an increase in the source resistance (R_s) at higher V_DS, known as an increase in the dynamic source access resistance. At higher gate voltages where carriers transverse the channel with a saturation velocity, the channel current continues to increase by populating more carriers at the channel surface but the ungated source region of the device cannot keep up with required carrier density, and with the saturated carrier velocity, the source resistance increases. This compromise between the channel current and the source resistance has been recently mitigated by introducing Fin-like channels that decrease the channel current and delay the impact of the source resistance on g_m-roll-off further extending the voltage ranges over which g_m is constant. Notably, Joglekar et al. utilized Fins with different widths yet with the same channel width for planar and for each set of Fin widths in a single high electron mobility transistor (HEMT) channel for g_m-compensation. However, in that work, the residual currents for each set of previously turned on Fins degrade the overall device current at higher gate voltages and lead to nonlinearities in the current–voltage characteristics. Additionally, the width of the g_m-plateau cannot
be substantially improved for large-signal operations with Fin-only architectures (due to limited tunability range for threshold voltage, \( V_T \)) and Schottky metal gates (which are susceptible to gate diode turn-on and large leakages at small positive \( V_G \)).

We synthesized planar HEMTs with multiple narrow Fin-HEMTs and incorporated a thin gate insulator to achieve high linearity, purely by adjusting the device layout using only a commercial Al\(_{0.23}\)Ga\(_{0.77}\)N/GaN-on-Si wafer without any additional epitaxial layer growth. The detailed fabrication process of AlGaN/GaN metal–insulator–semiconductor HEMTs (MIS-HEMTs) is described in the Supporting Information. Figure 1A shows top-view scanning electron microscopy (SEM) images of the synthesized device. The synthesized device consisted of a 10.3 μm wide planar region and 6, 11, 8, and 8 Fins for 160, 100, 80, and 50 nm Fin widths \( (W_{\text{Fin}}) \), respectively, under one gate electrode, in order to operate all the regions simultaneously and to achieve a highly linear transfer characteristic. The gate-to-source \( (L_{GS}) \), the gate-to-drain \( (L_{GD}) \) distances, and the gate length \( (L_G) \) are 0.5, 1.4 μm, and 90 nm, respectively. As can be seen in Figure 1B,C, a planar reference device fabricated on the same die shows a nonlinear drain current as \( V_G \) increases and the \( g_m \) roll-off.\(^{2,3}\) Additionally, the extracted unity current-gain frequency \( f_T \) also had a peak and decreased quickly as \( V_G \) increased, as shown in Figure 1D due to the inversely proportional dependence of \( f_T \) on \( R_s \).\(^{29}\) These nonlinearities are resolved for the synthesized device by the sequential turn-on of multiple channels that made the overall source resistance constant, as shown in Figure 1E,F for \( I_D-V_G \) and for \( g_m-V_G \) characteristics, respectively. Figure 1G shows the \( f_T-V_G \) characteristic, which is nearly constant for \( V_G > V_T \) for the synthesized device compared to a strongly peaked shape, congruent with the \( g_m-V_G \) curve, for the planar device.

Synthesis of the linear transistor was informed with the detailed characteristics of its individual components composed

Figure 1. Device structure and concept of the synthesized GaN MIS-HEMT device consisting of planar and multi-Fin regions, and its electrical characteristics compared to a conventional planar device. A gate length \( (L_G) \) of 90 nm, a gate width \( (W_G) \) of 20 μm, a gap between each Fin \( (W_{\text{gap}}) \) of 200 nm, and a drain to source distance \( (L_{DS}) \) of 2 μm were used for all devices in Figure 1 and Figure 2. (A) Top-view SEM images of the fabricated device showing a planar region and a Fin region under a single gate electrode. (B) Measured \( I_D-V_G \) (C) \( g_m-V_G \) and (D) \( f_T-V_G \) for a planar device. (E) Measured \( I_D-V_G \) (F) \( g_m-V_G \) and (G) \( f_T-V_G \) for the synthesized device.
of a fixed $W_{\text{Fin}}$ per device, in the range $50-200$ nm, denoted as individual Fin devices. A top-view SEM and cross-sectional high-resolution transmission electron microscopy (HRTEM) images in Figure 2A–C of the fabricated individual Fin device with $W_{\text{Fin}}$ of 100 nm show accurate alignments and good Fin formations with conformal dielectric (6 nm Al$_2$O$_3$ on 5 nm AlGaN barrier) and gate metal layers. The fabricated devices showed very steep subthreshold slopes with an average value of $83.6$ mV/dec across 20 devices with different $W_{\text{Fin}}$ from 50 to 200 nm and a planar device as shown in Figure 2D. The threshold voltage increased for smaller $W_{\text{Fin}}$ (Figure 2D,E), due to the deeper penetration of the sidewall electric field into the channel of narrower Fins. This side-gate effect was independent of GaN sidewall facet orientation of either a-plane $(11\overline{2}0)$ or m-plane $(10\overline{1}0)$ because of the nearly symmetric energy band structure of wurtzite GaN for $\Gamma-K$ and $\Gamma-M$ valleys at the lower conduction band and the nearly identical etch profile (and field-distribution) in our process for both types of facets.

The broad range of $V_T$ from $-5$ V for planar devices to $-0.5$ V for 50 nm wide Fins provides a tuning knob to synthesize a linear multichannel device, composed of sets of individual channels each with a given $V_T$, such that these sets of individual channels turn on sequentially. The properties of such a synthesized device can be expressed with the superposition of its individual components such that

$$I_{D,\text{total}}(V_G) = a_{I_D,0}(V_G - V_{T,0}) + a_{I_D,1}(V_G - V_{T,1}) + \ldots + a_{I_D,k}(V_G - V_{T,k})$$  \hspace{1cm} (1)$$

$$g_m,\text{total}(V_G) = a_{g_{m,0}}(V_G - V_{T,0}) + a_{g_{m,1}}(V_G - V_{T,1}) + \ldots + a_{g_{m,k}}(V_G - V_{T,k})$$  \hspace{1cm} (2)$$

$$g_m',\text{total}(V_G) = a_{g_{m,0}'}(V_G - V_{T,0}) + a_{g_{m,1}'}(V_G - V_{T,1}) + \ldots + a_{g_{m,k}'}(V_G - V_{T,k})$$  \hspace{1cm} (3)$$

where $a_k$ is the weight of $k$th channels for a family of Fins with a $W_{\text{Fin},k}$ and a $V_{T,k}$. $k = 0$ represents the planar device characteristics. Therefore, we have multiple knobs $W_{\text{Fin},k}$ through $V_{T,k}$ and $g_{m,k}$ and $a_k$ for engineering the linearity of the drain current of the synthesized device. We chose a planar device and 4 different Fin devices with $W_{\text{Fin}}$ of 160, 100, 80, and 50 nm because of their uniformly separated $g_m'$ curves, as
were observed at illustrating linear transfer characteristics over a wide of device for can be clearly observed in the uniformly distributed result in cancellation of nonzero powers.

higher drain biases that are suitable for delivering high output that the third-order nonlinearity caused by that the intended \( g_m' \) sweet spot at \( V_G = -2.62 \) V was clearly observed in the fabricated synthesized device, indicating that the third-order nonlinearity caused by \( g_m' \) will be completely canceled out, while the planar device does not have this sweet spot. It is worth noting that the breakdown voltage of this device was 54 V, as shown in Supplementary Figure 7, which ensures that the device can be operated at higher drain biases that are suitable for delivering high output powers.

We demonstrate next that this DC linearity translates to RF linearity with record performance. Small-signal S-parameter, single-tone continuous wave (CW) power sweep, and two-tone measurement were performed on the fabricated 4-Fin synthesized device with the same geometry (\( L_{G5} L_{GD} \) and \( L_{Gi} \)), but with T-gates that reduce the input impedance and air-bridges that connect parallel devices to reduce output impedance as illustrated in Figure 4A. We refer to this device as device A in the following discussions. The T-gate comprised a gate foot of 90 nm and a stem height and gate head length of 150 and 250 nm, respectively, as seen in Figure 4B, resulting in an extracted gate resistance of \( \sim 5 \) Ω. With the air-bridge connected devices (Figure 4C), the effective channel width was 107.2 μm (\( W_{eff} = W_{planar} + \Sigma W_{fin} = 13.4 \times 8 \)). The peak extrapolated values of \( f_T \) and the maximum oscillation frequency (\( f_{max} \)) were 71.3 and 123.4 GHz, respectively, at a DC bias point of \( V_D = 5 \) V and \( V_G = -4 \) V, as shown in Supplementary Figure 10. Parts D and E of Figure 4 are contour curves of the extracted \( f_T \) and \( f_{max} \) over the output characteristics of the device, illustrating broadly uniform \( f_T \) and \( f_{max} \) contours in most of the saturation region. The maximum stable gain (MSG) characteristics as a function of frequency without pad de-embedding is shown in Supplementary Figure 11, which illustrates suitability for proper operation in the mm-wave regime.

For all the linearity measurements at 5 GHz, the device was biased in class-A operation with \( V_D = 5 \) V and \( I_D = 52 \) mA. To examine the linearity performance of the device for large-signal power applications, a CW power sweep was performed at 5 GHz with the 50 Ω load to measure distortions to amplitude (AM-AM (\( |S_{21}| \))) and to phase (AM-PM (\( \angle S_{21} \))), as shown in Figure 4F. From the AM-AM distortion characteristics, the small-signal gain (\( |S_{21}| \)) was 8.44 dB for the synthesized device and 8.42 dB for the planar device. The relatively low gain was attributed to the use of a calibration plane located before the lossy input tuner, as described in the Supporting Information.
with Supplementary Figure 12. The output 1 dB gain compression point, $P_{1\text{dB}}$, was improved from 15.6 dBm for the planar device to 17.9 dBm for the synthesized device due to its enhanced $g_m$ linearity. The AM-PM distortion was reduced from 1.38° to 1.27° for the input power range of $-15$ to $+12.75$ dBm, suggesting a nearly voltage independent gate-to-source capacitance ($C_{gs}$) and a very small nonlinear contribution of the feedback capacitance ($C_{gd}$) into the input impedance of the device.33

The reduction in intermodulation distortion of the synthesized device was validated by a two-tone measurement with a center frequency ($f_0$) of 5 GHz and a tone spacing ($\Delta f$) of 10 MHz. The load impedance was fixed at 50 $\Omega$. Figure 4G shows the measured fundamental frequency signal power ($P_{f,0}$) at 5 GHz and the third-order intermodulation signal power (IM3) at 4.99 GHz as a function of one-tone power ($P_{\text{in}}$ per tone). The IM3 of the synthesized device was substantially improved by $-26$ dB at a $P_{\text{in}}$ per tone of $-8.5$ dBm from that of the planar device, because of the $g_m''$ canceling points introduced by various $V_T$, as noted in Figure 2G and Figure 3D. By linear extrapolation of OIP3 with a slope of 1:1 and 3:1 from $f_T$ and $f_{\text{max}}$ (Supplementary Figure 14), respectively, the peak OIP3 value was 40 dBm, resulting in a linearity figure of merit $OIP3/P_{\text{DC}} = 15.9$ dB, while those of the planar device were 27 dBm and 2.9 dB at this bias point. To the best of our knowledge, this value is the highest for any given discrete semiconductor transistor to date.10,11,19,22 Interestingly, deep IM3 sweet spots, which give a very high linearity at specific input power levels, can be introduced by only adjusting the gate bias, as shown in Figure 4H. These IM3 sweet spots for the synthesized device are closely correlated with the $g_m''$ sweet spots we intentionally introduced, when the quiescent gate
voltage is getting close to the $g_m$ sweet spot at $V_G$ of $-2.62$ V, as shown in Supplementary Figure 6, and disappear when the gate is biased far from it. The sweet spots for the different $V_G$ biases still follow the 3:1 slope from the low IM3 at $V_G = -3.0$ V, which consolidates the extrapolated OIP3 of the synthesized device for all measured conditions. Table 1 benchmarks the key linearity figures of merit for discrete GaN-based transistors.

Table 1. Comparison of Key Linearity Figures of Merit for Discrete GaN-Based Transistors

<table>
<thead>
<tr>
<th>reference</th>
<th>frequency (GHz)</th>
<th>OIP3 (dBm)</th>
<th>OIP3/P_{DC} (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2016 HRL w/o linearization (ref 11)</td>
<td>2</td>
<td>42</td>
<td>4.1</td>
</tr>
<tr>
<td>2008 FBH Berlin (ref 15)</td>
<td>2</td>
<td>54</td>
<td>10.1</td>
</tr>
<tr>
<td>2009 FBH Berlin (ref 16)</td>
<td>2</td>
<td>34</td>
<td>2</td>
</tr>
<tr>
<td>2005 HKUST (ref 17)</td>
<td>2</td>
<td>33</td>
<td>2</td>
</tr>
<tr>
<td>2017 MIT (ref 18)</td>
<td>6</td>
<td>36</td>
<td>2</td>
</tr>
<tr>
<td>2017 UCSB (ref 19)</td>
<td>10</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>2018 OSU (ref 20)</td>
<td>10</td>
<td>33</td>
<td>3.4</td>
</tr>
<tr>
<td>2019 OSU (ref 21)</td>
<td>10</td>
<td>33a</td>
<td>4.7a</td>
</tr>
<tr>
<td>2020 OSU (ref 22)</td>
<td>10</td>
<td>39</td>
<td>13.3</td>
</tr>
<tr>
<td>2018 NTU (ref 12)</td>
<td>10</td>
<td>32a</td>
<td>13.3</td>
</tr>
<tr>
<td>2019 Northrop Grumman (ref 13)</td>
<td>30</td>
<td>37</td>
<td>6</td>
</tr>
<tr>
<td>2019 UCSB (ref 14)</td>
<td>30</td>
<td>35</td>
<td>11.4</td>
</tr>
<tr>
<td>this work</td>
<td>5 (device A)</td>
<td>40</td>
<td>15.9</td>
</tr>
<tr>
<td></td>
<td>30 (device B)</td>
<td>&gt;31</td>
<td>&gt;8.2</td>
</tr>
</tbody>
</table>

We obtained these values by the same method of extraction presented in this manuscript even though the original manuscripts reported higher values.

In order to further corroborate the key device performance for its applications in mm-wave LNAs, a synthesized device, device B, with a shorter source-to-drain distance ($L_{SD}$) of 690 nm compared to $L_{SD}$ of 2 $\mu$m for device A was fabricated for the purpose of obtaining a higher $g_m$, a reduced knee voltage, and lower drain bias operation, and it was characterized at 30 GHz. The measured DC characteristics are shown in Supplementary Figure 16. As shown in Figure 5A, device B has a shorter $L_{GS}$ and $L_{GD}$ distance of 250 and 350 nm, respectively, but the same gate length of 90 nm. Both devices A and B were otherwise identical and were fabricated on the same die. Device B was biased at $V_D = 3$ V and $I_D = 63$ mA in the following single-tone CW power sweep and two-tone linearity measurements. The source and load impedances were matched to conjugate of the input impedance of the device ($\Gamma_{in}$) and 0.17 $\angle$104°, respectively, for the best linearity. As can be seen in Figure 5B, the single-tone CW power sweep measurement shows the maximum $P_{out}$, linear gain, $P_{1dB}$, and the peak power added efficiency (PAE) of 19.6 dBm, 7.52 dB, 17.8 dBm, and 32.3%, respectively. From the two-tone linearity test, the input third-order intercept point (IIP3) of 23.5 dBm, OIP3 of 31 dBm, and OIP3/P_{DC} of 8.2 dB were estimated as lower bounds by linear extrapolation with a 1:1 slope and a 3:1 slope at the lowest available $P_{in}$ (not as low as in Figure 4), as shown in Figure 5C. Since the noise characteristic is another key parameter for LNAs, on-wafer noise figure measurement was also carried out. An automated source-pull with the 50 $\Omega$ load was used to find the optimum source impedance ($\Gamma_{s,opt}$) for the minimum noise figure (NF_{min}) with varying frequencies from 8 to 50 GHz and the drain current. Figure 5D exhibits the measured NF_{min} and the associated gain ($G_a$) as a function of frequency with $V_D = 5$ V and $I_D = 45$ mA showing the NF_{min} of 2.2 dB at 30 GHz. Measured NF_{min}, gain, and IIP3 at 30 GHz versus the drain current are shown in Supplementary Figure 17. In order to compare the performance of our device with Table 1. Comparison of Key Linearity Figures of Merit for Discrete GaN-Based Transistors

![Figure 5. Device B for LNA applications. (A) Schematic illustration of device B structure with a short gate-to-source ($L_{GS}$) of 250 nm and a gate-to-drain length ($L_{GD}$) of 350 nm, but the same gate length of 90 nm. (B) The single-tone CW power sweep and (C) the two-tone linearity measurements were performed at $V_G = 3$ V ($I_D = 63$ mA). The tone spacing for the two-tone measurements was 10 MHz. (D) Noise measurements with the optimum source impedance ($\Gamma_{s,opt}$) for the minimum noise figure (NF_{min}) and the 50 $\Omega$ load, but varying measurement frequency from 8 to 50 GHz.](https://dx.doi.org/10.1021/acs.nanolett.0c00522)
Table 2 summarizes major parameters for LNAs with diverse other state-of-the-art mm-wave LNAs, the dynamic-range figure-of-merit (DR-FOM) was calculated as follows:

$$DR - FOM = \frac{\text{OIP3}}{(F - 1)P_{DC}}$$

where $F$ is the noise factor, $F = 10^{NF/10}$, and note that OIP3 is the multiplication of IIP3 and power gain ($\text{OIP3} = \text{IIP3-Gain}$).

Table 2 summarizes major parameters for LNAs with diverse available technologies above 20 GHz, such as GaN-based devices, commercialized GaAs pseudomorphic HEMTs (pHEMTs) and SiGe BiCMOS (BiCMOS), which clearly indicates our proposed device has a great potential for mm-wave LNAs.

In conclusion, the new concept of an intrinsically synthesizable linear device was implemented by changing only the device layout. The design can be transferred to other heterostructure material combinations such as InAlAs/InGaAs, In(Al)N/GaN, the graded channel, the superlattice multi-heterostructure material combinations such as InAlAs/InGaAs, only the device layout. The design can be transferred to other materials.

**ASSOCIATED CONTENT**

**Supporting Information**

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.0c00522.

Detailed information regarding the device fabrication steps, the detailed methods of linearization for transfer characteristics with supplementary Table 1, the layout of the synthesized device, the device measurements and characterization (DC and breakdown characteristics of the synthesized device, extraction of $f_T$ and $f_{max}$ extrinsic RF characteristics, the de-embedding methodology, two-tone intermodulation linearity performance), the selection of the optimum bias point for high linearity performance, the load-pull measurement at 30 GHz, the noise parameter measurement at 30 GHz (PDF)

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**Author Contributions**

S.A.D. conceived the synthesized device, led the project, and cowrote the manuscript. W.C. developed the synthesis approach, designed, fabricated, and measured the devices and wrote the manuscript. R.C. developed the fabrication process for the devices together with W.C. who further developed the T-gate and air-bridge devices. R.C. performed the TEM characterization. A.T. and R.L. contributed to the development of device fabrication. C.L. and W.C. performed all the characterization, de-embedding, and analysis of the results at 5 GHz. V.B. and W.C. performed measurements at 30 GHz and W.C. performed the analysis. P.M.A. led the RF and mm-wave characterization and analysis and coled the project. All authors contributed to the manuscript writing.

**Notes**

The authors declare the following competing financial interest(s): UC San Diego has filed a patent application (PCT/US2018/058407) on the synthesized planar, multi-Fin device.

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part at the CINT, U.S. Department of Energy, Office of Basic Energy Sciences User Facility at Los Alamos National Laboratory (Contract No. DE-AC52-06NA25396) and Sandia National Laboratories (Contract No. DE-AC04-94AL85000). This work was performed in part at the San Diego Nanotechnology Infrastructure (SDNI) of UCSD, a member of the National Nanotechnology Coordinated Infrastructure, which is supported by the National Science Foundation (Grant ECCS-1542148). W.C. was partially supported through the University of California Center for Design-Enabled Nanofabrication (C-DEN). This work was supported in part by an NSF-ECCS award #1711030 concerned with integration of vertical power devices on Si.

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Supporting Information:

An Intrinsically Linear Transistor for Millimeter-Wave Low Noise Amplifiers

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Keywords: Linear, GaN, mm-wave, low noise amplifier

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IV. References
I. Device fabrication:

The overall process flow is illustrated in Supplementary Fig. 1. A commercial \( \text{Al}_{0.23}\text{Ga}_{0.77}\text{N/GaN-on-Si} \) wafer was used. After solvent and Piranha treatment for a clean surface, the initially grown 25 nm AlGaN barrier layer was thinned down to 5 nm by \( \text{BCl}_3/\text{Cl}_2 \) reactive ion etching (RIE) with a plasma power of 50 W. Alignment markers are first patterned by a positive photoresist, AZ12XT-5, and a 600 nm trench was etched by the same \( \text{BCl}_3/\text{Cl}_2 \) RIE etch chemistry. Then, an Ohmic contact process followed. A Ti/Al/Ni/Au(=20/120/40/50 nm) metal stack was evaporated, lifted off, and annealed at 875 °C for 30 sec to make Ohmic contact. A sheet electron concentration of \( 9.9\times10^{12} \text{ cm}^{-2} \) and an electron mobility of \( 1124 \text{ cm}^2/\text{V} \cdot \text{s} \) were extracted from the Hall-effect measurement after AlGaN barrier thinning. The contact resistance, \( R_C \), was 0.47 Ω-mm measured by the Transmission line method (TLM). A 740 nm-thick Fox16 hydrogen silsesquioxane (HSQ) was coated, soft-baked at 180 °C for 2 min, and patterned by e-beam lithography with an optimized proximity effect correction to pattern uniform Fin structures. After 5 min UV-ozone exposure to harden the patterned HSQ layer, Fin etching was performed with \( \text{BCl}_3/\text{Cl}_2 \) RIE, and the HSQ layer was removed by dipping into a 1:20 diluted buffered oxide etchant (BOE). A surface cleaning step by a 29% \( \text{NH}_4\text{OH} \) solution with sonication for 15 min was carried out \(^1\), and the sample was then immediately loaded to Beneq TFS200 atomic layer deposition (ALD) system. 20 cycles trimethyl aluminum (TMA) pre-pulse and 45 cycles of \( \text{Al}_2\text{O}_3 \) deposition process were performed at a chuck temperature of 200 °C. No post-deposition annealing for the gate insulator was performed. For rectangular gate devices, an MMA/PMMA double layer was used and a Ti/Au layer of 20/80 nm was evaporated. For T-gate devices, a Ti/Au of 50/400 nm metal stack was evaporated by a conventional ZEP/PMGI/ZEP tri-layer electron beam lithography process \(^2\). After opening ohmic contact windows by RIE, a Ti/Au of 50/400 nm, was deposited by e-beam evaporation, and
followed by lift-off. For air-bridges, a 2.7 μm-thick MMA copolymer layer was used as a temporary supporting material, and a total 1.2 μm-thick Ti/Au layer was deposited and lifted-off by an image reversal photoresist and a directional sputtering without rotation. Finally, after in-situ N₂ plasma for 2 min with a RF power of 20 W by plasma-enhanced chemical vapor deposition (PECVD) at 200 °C, a 60 nm Si₃N₄ layer was deposited as a passivation layer. No pad opening was performed, and all the measurements were carried out by penetrating the passivation layer by probe tips.

II. Linearization of Transfer Characteristics and Synthesized Device Layout Design:

The detailed linearization and device design procedure is as follows:

First, transfer characteristics of planar and individual Fin devices were measured and differentiated with respect to \( V_G \) to obtain \( g_m' - V_G \) curves. All devices had a fixed \( W_G = 20 \) μm. A fixed spacing between the Fins, \( W_{gap} = 200 \) nm, was used. Therefore, each Fin device was composed of a different number of Fins, \( N_{Fin} \), in the 20 μm wide channel.

Second, planar devices and Fins with different widths (\( W_{Fin} \)) have flat \( g_m \) regions over a narrow \( V_G \) that shifts to positive \( V_G \) as \( W_{Fin} \) decreases. \( W_{Fin} \) were then selected to superimpose the flat \( g_m \) regions over the widest possible \( V_G \) for linearization. Here, we chose a \( V_G \) range from -4 V to 2 V and \( W_{Fin} \) of 160, 100, 80, and 50 nm.

Third, as can be seen in Supplementary Fig. 3 top panel, the peak of \( g_m' \) was determined for the device with \( W_{Fin,1} = 160 \) nm (\( P_1 = 2.4 \) mS/V), along with the \( g_m' \) value of the planar device (\( N_1 = 0.4 \) mS/V) at the same \( V_G \). We divide \( P_1 \) by \( N_1 \) to obtain the absolute ratio, \( R_1 \).

Fourth, a new \( g_m' - V_G \) curve with calculated \( R_1 \) as \( g_{m,1 - Fin - synthesized} = g_{m,planar}' + R_1 \cdot g_{m,160}' \) was then calculated and plotted.
Fifth, steps 3) and 4) with the synthesized $g_m'$ and that of the chosen narrower Fins were then repeated for the 100, 80, and 50 nm Fins.

Sixth, additional corrections to the factors $R_1$ to $R_4$ is needed to null the cumulative $g_m$ variation, $\Delta g_m = \int_{-4}^{2} g_m' dV_G$. A Factor F is introduced (Supplementary Fig. 4A). Note that $\alpha_0 = 1$ for the planar device which is chosen as the reference for $g_m$ correction.

Seventh, step 6) was repeated by varying $F$ to find the optimal $F$ which made $g_m'$ ripples centered at zero, resulting in the minimum possible $\Delta g_m$. As shown in Supplementary Fig. 4, we obtained the optimal $F=1.35$ and $\Delta g_m=-0.7 \mu S$.

Eighth, the optimal $\alpha_1$ to $\alpha_4$ were then calculated by multiplying $R_1$ to $R_4$ with the optimal $F$. We then multiplied the number of Fins ($N_{Fin}$) that were present in the reference Fin devices with $W_G=20 \mu m$ by the optimal $\alpha_1$ to $\alpha_4$, and rounded the obtained fractional number, noted as $A_k$ to obtain the final number of Fins – per Fin width – in the synthesized device. $A_k=\alpha_k \times N_{Fin,k}$.

Ninth, By considering the gap between each Fin ($W_{gap}=200 \text{ nm}$), we calculated the total device width ($W_{total}$) including $W_{gap}$: $W_{total} = W_{planar} + \sum_{k=1}^{4} (W_{Fin,k} + W_{gap}) \times A_k$. Here, $W_{total}=38.69 \mu m$.

Tenth, however, we wanted to fix the etched GaN mesa region width to 20 $\mu m$ so that the final devices have a minimal gate metal resistance $R_g$. Therefore, we normalized all device dimensions to 20 $\mu m$. Then resulting planar device width was $20 \times \frac{20}{38.69} = 10.3 \mu m$, and the final Fin numbers were 6, 11, 8, and 8 for $W_{Fin}$ of 160, 100, 80, and 50 nm obtained by multiplying $A_k$ by the width ratio, $A_k \times \frac{20}{38.69}$, and rounding the obtained number.

All the calculated values are summarized in Supplementary Table 1.
Supplementary Fig. 5 shows the transfer characteristics for the designed device based on the above described procedure together with that of the fabricated 4-Fin synthesized devices. The derivatives of the transfer characteristics are also shown. There is a small difference in the transfer characteristics between the designed and fabricated device embodied in a slight positive shift of the threshold voltage. This is most likely due to the fact that the calibration devices used in the design phase were completed in whole at the Center for Integrated Nanotechnologies (CINT) cleanroom in Albuquerque, whereas the synthesized device was completed at the nano3 facilities at UCSD including most importantly the pre-ALD TMA pre-pulsing and Al₂O₃ deposition (e-beam lithography, for the Fins only, was performed at CINT).

III. Device Measurements and Characterization:

In order to measure DC as well as on-wafer RF performance of the devices, all the device layout in this work was based on ground-signal-ground (GSG) structures. For DC characteristics of the individual devices with fixed Fin widths – devices with only one finger – were measured by an Agilent B1500A system. Only for the DC characteristics of the 8-finger device in Figure 4D, 4E (solid lines), and Supplementary Fig. 8, an Agilent E3631A DC power supply was used and automatically controlled by a separate laptop and a GPIB cable, primarily due to the current compliance of 100 mA in our B1500A system, while the drain current of the 8-finger device exceeded this limit.

On-wafer small-signal characteristics of the device were measured by an Agilent N5242A vector network analyzer (VNA). For small-signal characteristics to extract \( f_T \) and \( f_{\text{max}} \), the VNA was calibrated up to the input and the output GSG probe tips by a CS-5 SOLT calibration substrate. S-parameters were measured from 100 MHz to 26.5 GHz with an intermediate frequency (IF) bandwidth of 15 kHz and 5-times averaging in the VNA setup. For the de-embedding of pad
parasitic, open and short patterns on wafer as can be seen in Supplementary Fig. 9, were used to characterize the parallel and the series parasitics, respectively. With the measured Y-parameters of the open and short patterns, the actual transistor Y-parameters can be obtained from 3:

\[ Y_{\text{trans}} = \left( (Y_{\text{dut}} - Y_{\text{open}})^{-1} - (Y_{\text{short}} - Y_{\text{open}})^{-1} \right)^{-1}, \tag{6} \]

where \( Y_{\text{trans}} \) is the de-embedded transistor Y-parameters, \( Y_{\text{dut}} \), \( Y_{\text{open}} \), and \( Y_{\text{short}} \) are Y-parameters obtained from the measured S-parameters of the device, open, and short patterns, respectively. Then, the \( Y_{\text{trans}} \) was transformed to h-parameters, and \( |h_{21}| \) was used for \( f_T \) extraction from the 20 GHz point with a slope of -20 dB/dec (Supplementary Fig. 10). For \( f_{\text{max}} \) extraction, the unilateral power gain, \( U \), was calculated with the following equation 4:

\[
U = \left( \frac{S_{21}}{S_{12}} - 1 \right)^2 \times \left( k \times \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|^2} \right), \tag{7}
\]

where \( k = \frac{1}{2} \left( \frac{S_{21}}{S_{12}} - \text{Re}\left( \frac{S_{21}}{S_{12}} \right) \right) \).

Similar to the \( f_T \) extraction, \( f_{\text{max}} \) was linearly extrapolated from the 20 GHz point with a slope of -20 dB/dec.

Supplementary Fig. 12 illustrates the measurement setups for each RF linearity characterization and calibrations. For the single-tone continuous wave (CW) power sweep measurement, a Maury Microwave 1643N manual slide-screw tuner was used for input impedance matching. No tuner was used at the output of the device corresponding to the 50 Ω load. For the CW power sweep, under the DC bias condition \( (V_D=5 \text{ V and } I_D=52 \text{ mA}) \), the tuner position was set by watching \( S_{11} \) in the VNA screen to make it zero as close as possible, then the tuner position was not changed until all the measurement was finished. After finding the optimal tuner position for input matching of the device, 10 dB attenuators were specified for the ports in the VNA setting to prevent RF power overloading. The VNA power was calibrated up to the input bias-T by
connecting a power meter, Agilent N1911A, for an input power range of -15 dBm to +15 dBm with a step of 1 dBm at a fixed frequency of 5 GHz, and S-parameters were calibrated by an electronic calibration module, N4691-60004. Then, the calibrated input and output bias-Ts were connected to the input tuner and the drain probe tip. Finally, a CW input power was swept from -15 dBm to +12.75 dBm, and S-parameters were measured and recorded by the VNA.

For the two-tone measurement, the same tuner, Maury Microwave 1643N, was used for input impedance matching, and no tuner was used at the output of the device corresponding to the 50 Ω load. In order to calibrate the power of the input and the output RF signal accurately, two directional couplers, Mini-circuits ZADC-10-63-S+, were installed at the input and the output bias-Ts, and connected to the two-channel power meter, Agilent E4419B as illustrated in Supplementary Fig. 12. For two-tone signal generation, two Agilent N5182A MXG vector signal generators were used for 5 GHz and 5.01 GHz, and two signals were combined by a power splitter, HP 11667B. For observing the difference of output two-tone signals, an Agilent N9020A MXA signal analyzer was used. The input two-tone signal power from the signal generator was increased and the power of 5 GHz signal and 4.99 GHz at the signal analyzer, were simultaneously recorded. From these recorded values and assuming that the total output RF power is dominated by two fundamental signal powers, \( P_{f,0} \) and IM3 at each \( P_{in} \) per tone were calculated as follows:

\[
\begin{align*}
P_{in\ per\ tone\ (dBm)} &= P_{Ch,A} - 3 \\
P_{f,0\ (dBm)} &= P_{Ch,B} - 3 \\
IM3\ (dBm) &= P_{f,0} - (IMR_3)
\end{align*}
\]

where \( P_{in\ per\ tone} \) and \( P_{f,0} \) are the powers of fundamental signal per tone at the input and output, respectively; \( P_{Ch,A} \) and \( P_{Ch,B} \) are the measured total RF power from the power meter for the input and output, respectively; IM3 is the 3\textsuperscript{rd}-order intermodulation power, and IMR\(_3\) is the difference between the signal powers of 5 GHz and 4.99 GHz from the signal analyzer.
III.A. Optimum Bias Point for the High Linearity Performance:

In order to find the optimum bias point of the synthesized device, two-tone measurements were performed by varying the DC bias point. During this measurement, the RF power at both signal generators was fixed at -2 dBm which resulted in an actual measured power per tone (P\text{in} per tone) of -10.5 dBm read by the power meter, the input tuner position was also not changed, and IMR\text{3} from the signal analyzer was recorded with varying the DC bias point. The gate voltage was changed from -4 V to -2 V with a step of 0.1 V, and the drain voltage was swept from 2 V to 5 V with a step of 0.5 V. Recorded IMR\text{3} values are plotted as a 2D contour plot in Supplementary Fig. 13, the highest IMR\text{3} of 85.1 dBc was achieved at $V_D$=5 V, $V_G$=-3 V, and $I_D$=52 mA. At this quiescent point, the RF input power at the signal generator was swept from -3 dBm to 15 dBm which resulted in P\text{in} per tone of -11.5 dBm to 6.5 dBm for extractions of output 3\textsuperscript{rd}-order intermodulation points (OIP3) for the synthesized and planar devices. Supplementary Fig. 14 (a) and (b) illustrate the linear extrapolation of OIP3 with a slope of 1:1 from each P\text{f,0} point and 3:1 from each IM3 point for the synthesized and planar devices. The average of 5 points of plotted OIP3 for the synthesized device was 39.3 dBm with a peak value of 39.8 dBm. Supplementary Fig. 14 (c) and (d) show the two-tone spectra of the two devices at P\text{in} per tone=-8.5 dBm, and IMR\text{3} was clearly reduced by 26.1 dB. For reference, a planar device with the total gate width of 80 μm (20 μm × 4) was used to in order to match the DC power and $g_m$ and the small-signal RF gain to that of the synthesized device for a fair comparison. The DC output characteristics of the planar device are shown in Supplementary Fig. 15.

III.B. Load-pull measurement at 30 GHz:

Large signal characterization was performed using single tone and two-tone vector receiver load-pull measurements at Ka band. The setup shown in Supplementary Fig. 21 was realized using
Maury Microwave LXI 8-50 GHz compliant automated tuners, low loss couplers, broadband amplifiers, Keysight PNAX and bias-tees with the entire system being controlled using IVCAD software suite.

Vector receiver load-pull methodology allows accurate large signal characterization of transistors using the narrow band VNA receiver paths instead of mean power measured using a wideband power sensor. Power waves \((a_1, b_1, a_2, b_2)\) can be directly measured at the VNA receivers through the external input and output bidirectional couplers providing real time input Gamma, \(\Gamma_{IN} = \frac{b_1}{a_1}\), and load Gamma, \(\Gamma_{LOAD} = \frac{a_2}{b_2}\), as shown in Supplementary Fig. 21 (a). This allows for accurate calculation of delivered input power, \(P_{in,delivered} = \frac{1}{2}(|a_1|^2 - |b_1|^2)\), and subsequently, power added efficiency, \(PAE = \frac{(P_{out} - P_{in,delivered})}{P_{DC}} \times 100\).

System calibration involves performing 2-port calibration at the DUT plane, as shown in Supplementary Fig 21 (b), followed by 1-port power calibration for amplitude correction using power sensor, see Supplementary Fig. 21 (c). The attenuators on the coupled ports ensure that the VNA receivers don’t get compressed and operate in the linear region. During calibration, IVCAD provides an option to control the internal combiner to combine the two internal sources of the PNA-X allowing seamless switching between single and two-tone measurements.

System validation was performed by measuring a thru pattern and verifying that the variation in operating power gain, \(G_p = \frac{P_{out}}{P_{in}}\), across various impedance states on Smith Chart was within \(\pm 0.2\)dB.
Supplementary Fig. 21 (d) shows the final setup used for DUT measurement. Input Amplifier was chosen to provide sufficient drive power to drive DUT. DC biasing was provided using AMCAD 3200 PIV power supply.

**III.C. Noise Parameter Measurement at 30 GHz:**

Noise parameters extraction and measurements were performed using technique described by G. Simpson et al.,\(^5\) using an over determined data set of noise power measured at pre-characterized source gamma states. The setup shown in Supplementary Fig. 22 was realized using Maury Microwave 8-50 GHz LXI compliant automated tuner, Noise Source module which includes bias tee and switch, Noise receiver module which includes bias tee, switch and pre-amplifier, Keysight PNAX with direct receiver access, 4142B power supply and 11713B switch controller with the entire system being controlled using Maury ATS software suite.

System S-parameters calibration involves performing 2-port S-parameters calibration at the DUT plane, 1-port \(S_{22}\) calibration at noise source plane to calculate the S-parameters from the noise source to the DUT and tuner characterization at pre-determined impedance states. This is followed by system noise receiver calibration on a thru pattern to extract system noise parameters. During calibration, ATS provides an option to select different gain settings of internal pre-amplifier of PNAX noise receiver. This allows the user to select the appropriate gain setting during DUT measurement, thus avoiding receiver overload.

System validation was performed on a 3 dB on-wafer attenuator where the extracted \(\text{NF}_{\text{min}}\) was found to be similar with the attenuation value.
References:


(2) Wakita, A. S.; Su, C.-Y.; Rohdin, H.; Liu, H.-Y.; Lee, A.; Seeger, J.; Robbins, V. M.


Supplementary Fig. 1.
Schematic illustration of the device fabrication process.
Supplementary Fig. 2.
Measured $g_m-V_G$ and $g_m'-V_G$ of the fabricated planar device showing a $g_m$ roll-off corresponding to negative $g_m'$ and $\Delta g_m$. Note that $g_m'$ curve is 7-point averaged.
Supplementary Fig. 3.
Linearization of transfer characteristics by using $g^\prime_m-V_G$ and determining the weights of numbers of each Fin.
Supplementary Fig. 4.

(a) A weighting factor $F$ was used to lift up the curve to make the center of $g_m'$ ripple at zero. (b) $\Delta g_m - F$ showing the optimum value of $F$. (c) $g_m' - V_G$ after Fin synthesizing by minimizing $\Delta g_m$ from $V_G$ of -4 V to +2 V.
Supplementary Fig. 5.

$I_D-V_G$, $g_{m}-V_G$, $g_{m}'-V_G$, and $g_{m}''-V_G$ characteristics of designed (based on experimental results of planar and individual Fin devices) and fabricated 4-Fin synthesized devices, showing a good agreement.
Supplementary Fig. 6.

$g_m''-V_G$ characteristics of the fabricated 4-Fin synthesized and planar devices (inset: zoomed-in plot around the $g_m''$ sweet spot at -2.62 V).
Supplementary Fig. 7.
Breakdown characteristics for the synthesized device.
Supplementary Fig. 8.
DC characteristics of the 8-finger synthesized device used for linearity measurements. (a) $I_D-V_G$, (b) $g_m-V_G$, and (c) $I_D-V_D$ characteristics measured by a DC supply.
Supplementary Fig. 9.
De-embedding patterns for (a) open, and (b) short configurations.
Supplementary Fig. 10.
Measured intrinsic small-signal characteristics of the fabricated device (Fig. 4). $h_{21}$ and $U$ were used for $f_T$ and $f_{max}$ extraction.
Supplementary Fig. 11.
Extrinsic maximum stable gain (MSG), $h_{21}$, and $U$ without pad de-embedding as a function of frequency demonstrating proper operation in the mm-wave regime.
Supplementary Fig. 12.
Block diagram of the on-wafer CW power sweep and two-tone measurement setup showing the calibration planes. (a) VNA power calibration, (b) VNA S-parameter calibration, (c) CW power sweep measurement setup. (d) Power calibration for the input and output up to bias-Ts, (e) two-tone measurement setup.
Supplementary Fig. 13.

Measured IMR$_3$, the difference between the signal powers of 5 GHz and 4.99 GHz from the signal analyzer, contour plots on the measured output characteristics of the synthesized device. The maximum IMR$_3$ of 85.1 dBc was achieved at $V_D=5$ V and $I_D=52$ mA.
Supplementary Fig. 14.

Measured two-tone intermodulation linearity performance of (a) synthesized device and (b) planar device. $P_{f0}$, IM3, and OIP3 are plotted as increasing $P_{in}$. 1:1 slope (black) and 3:1 slope (red) lines are shown to illustrate the extracted OIP3 points. Measured two-tone spectra of (c) synthesized device and (d) planar device to show IMR$_3$ reduction at the same RF input power.
Supplementary Fig. 15.
DC characteristics of a reference planar device used for linearity measurements. (a) $I_D-V_G$, (b) $g_m-V_G$, and (c) $I_D-V_D$ characteristics measured by a DC supply.
Supplementary Fig. 16.
DC characteristics of Device B with the synthesized Fin structure. (a) $I_D$-$V_G$ and $g_m$-$V_G$, and (b) $I_D$-$V_D$ characteristics measured by a DC supply.
Supplementary Fig. 17.
The minimum noise figure, gain, and IIP3 characteristics of the scaled synthesized device with varying drain current.
Supplementary Fig. 18.
Block diagram of the on-wafer Vector Receiver single and two-tone load-pull measurement setup showing the calibration planes. (a) Concept of Vector Receiver Load Pull, (b) 2 port vector receiver DUT plane calibration, (c) 1 port power calibration for amplitude correction using power sensor, (d) DUT measurement setup where port 1 can generate both single tone signal from the main source and two tone signals from the two internal sources combined by the internal combiner.
Supplementary Fig. 22.
Block diagram of the on-wafer noise parameter measurement setup showing the calibration planes.
| $V_G$ (V) | -3.3 | -2.35 | -1.45 | -0.6 | $|\text{Ratio}|$ ($R_L$) | Weight ($\alpha_{\text{m}}R_L \times F$) ($F=1.35$) | # of fins ($N_{\text{m}}$) in individual devices ($W_G=20 \mu$m) | Product ($A_{\text{m}}\alpha_{\text{m}} \times N_{\text{m}}$) (rounded) | Normalized # of fins in the synthesized device ($W_G=20 \mu$m) |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Planar | -3.98E-04 | - | - | - | 1 | 1 | 1 | 1 | 10.3 µm |
| 160 nm | 2.40E-03 | - | - | - | 0.17 | 0.22 | 50 | 11 | 6 |
| 1-Fin synthesized | - | -7.34E-04 | - | - | - | - | - | - | - |
| 100 nm | - | 2.54E-03 | - | - | 0.29 | 0.39 | 55 | 21 | 11 |
| 2-Fin synthesized | - | - | 4.52E-04 | - | - | - | - | - | - |
| 80 nm | - | - | 2.49E-03 | - | 0.18 | 0.25 | 66 | 16 | 8 |
| 3-Fin synthesized | - | - | - | -3.09E-04 | - | - | - | - | - |
| 50 nm | - | - | - | 2.24E-03 | 0.14 | 0.19 | 80 | 15 | 8 |

**Supplementary Table 1.**

Summary of the factors used in the procedure to determine the numbers of Fins for the synthesized device in a $W_G=20 \mu$m.